SILICON PROCESSING FOR MICROFLUIDIC NEUROPROBES

BY

OSCAR SIDA BI

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2018

Urbana, Illinois

Adviser:

Professor Yurii Vlasov

Abstract

Neural circuit processing is a poorly understood area of biology, but is critical to the development of novel biotechnologies for neurological disorders and neural networks for machine learning. One approach to overcome this deficiency in knowledge is to treat the brain as a black box that can be reverse engineered when known inputs are applied and measurable outputs are obtained. The most important measure in this system is the concentration profile of neurochemicals as they are the basis of all neural activities. To obtain these measurements in awake subjects, a neuroprobe capable of extracting neuromodulators with high temporal and spatial resolution and high chemical sensitivity and selectivity is needed. In addition, the overall dimensions of the probe must be minimized to limit brain tissue damage.

This thesis describes the fabrication process of a novel microfluidic-based neuroprobe capable of obtaining neuromodulators with high spatial and temporal resolution with limited tissue damage. This is achieved through the use of microfluidic channels with dimensions in the range of tens of microns, which is 100 times smaller than channels used today. The probe is made of silicon using standard processing techniques. It is shown that surface microfluidic channels with dimensions of 1.2μm wide and 700nm high are capable of being fabricated. Fabrication processes of silicon-based neuroprobes with needles of 55μm in width and 15μm in height are also discussed in detail. Packaging processes for the neuroprobe with plumbing systems are also developed and described in this work.

The silicon processing steps and packaging method described in this thesis will help lead to the completion of the high-performing silicon-based neurochemical probe that will aid in unlocking the mechanisms of neural circuits.

To my parents: My success is impossible without your sacrifices, support, and, above all, love.

Acknowledgments

I would like to begin by thanking my thesis advisor, Professor Yurii Vlasov, for providing me the opportunity to participate in the project described in this thesis. His wisdom and down-to-earth approach to research and engineering made a lasting impression that I will carry throughout my professional career. I would also like to acknowledge the financial support given by grant 1UF1NS107677-01 from the U.S. Department of Health and Services' National Institutes of Health (NIH).

This project would not be possible without the joint efforts from my fellow students and colleagues: Dr. Ryan Loh, Ari Esters, Yifei Yan, and Yan Zhang. I enjoyed our brainstorming sessions and appreciated your invaluable inputs to the design of the project. Special thanks to Ari Esters who took the lead in the development and fabrication of bulk silicon channels essential for the work presented in this thesis.

To the staff of the ECE supply center, ECE machine shop, and MNTL and MNMS cleanrooms, especially Dr. Glennys Mensing: Your help and guidance were critical to all the work I have done in my graduate study. Credit is also given to Purdue's Birck Nanotechnology Center for providing fabrication services for parts of the project.

I would also like to thank my parents for their unending support throughout my life. Without your vision and the invaluable opportunities you provided early in my life, I would not have succeeded in my academic journey. I owe both of you everything.

Last, but definitely not least, I would like to thank all my friends who were with me throughout my time at the University of Illinois. Thank you Tianxi Zhao, Ruizhong Zhang, Yu Huang, You Guang, Nathaniel Renner, Rachel Ziegler, Tyler Graham, and many others for making these past seven years some of the best times of my life. I will forever cherish our friendship and wish you all the best of luck in your future endeavors.

Table of Contents

Chapter 1: Introduction

With the increasing pace of technological advancements, especially in the fields of machine learning and biotechnology, it has become imperative that new and improved understanding of neural circuits is gained. New insights into cortical functions will allow for the development of novel drugs for treatment of various neural disorders and help improve the design of neuromorphic electronic circuits and neural networks used prevalently in machine learning and artificial intelligence.

One approach to gain insights into neural circuits is to treat the brain of an animal as a black box. Providing known inputs to the brain and obtaining measurable outputs allows the reverse engineering of neural circuits. For this model to provide meaningful results, detection of neural signals must be obtained in the brain of awake and behaving animals. While electrophysical neural probes capable of in vivo measurements are prevalent in the market, there is a deficiency of such neuroprobes for the detection of neurochemicals' spatial and temporal concentration transients in the brain. The ability to detect neurochemicals involved in cell-to-cell signaling is of essential importance as it is the fundamental basis for all communication within the brain including through synaptic cleft, glia-neuron communication, or through a volume extra-synaptic transmission by long-range diffusion [1]-[4].

The project presented in this thesis aims to rectify this deficiency through the development of a highly sensitive microfluidic-based neuroprobe capable of simultaneous extraction of several neurochemicals in the brain extracellular space (ECS) in awake and behaving animals with sub-second temporal and sub-100μm spatial resolution.

Chapter 2: Background

Neurochemical probes are evaluated by five major parameters: temporal resolution, spatial resolution, chemical sensitivity, chemical selectivity, and invasiveness. These criteria also constitute the major engineering tradeoffs in designing any implantable neuroprobe. Existing detection of neurochemicals in in-vivo environment revolves around four main technologies: optical sensing, electrochemical sensing, push-pull diffusion, and microdialysis.

Optical methods, such as cell-based neurotransmitter fluorescence engineered reporters (CNiFERs) [5] and genetically encoded fluorescent indicators [6]-[8], involve fluorescent imaging of the brain to monitor neurotransmitter receptor activation in in-vivo environment. Although these optical methods offer good chemical, spatial, and temporal resolution, and are non-invasive, they are finely tuned to the detection of a specific neuromodulator limiting their ability to monitor multiple neuromodulators simultaneously. In addition, these methods are restricted to work only on special genetic manipulations thus significantly reducing their versatility.

Electrochemical sensing measures neurochemicals using microelectrodes [9]. These electrodes can be either fabricated and multiplexed on silicon-based neuroprobes or solid electrodes such as metal wires or carbon fibers insulated with glass. These electrodes can be set up to optimize one or two of the essential parameters but are generally limited in their selectivity and/or resolution. The most popular method is fast-scan cyclic voltammetry (FSCV) that takes advantage of oxidation/reduction responses of neurochemicals at an electrode [10]. FSCV provides high temporal (<1 second) and spatial (<1μm) resolution and can be made to minimize tissue damage depending on the size of the electrodes. FSCV, however, only works on a small number of neuromodulators that have electroactive responses. The results from these measurements also suffer from presence of strong background noise from other electroactive metabolites and temporal pH drifts degrading the limit of detections (LOD) to nanomole range [11]. The process is also time-consuming due to the need for analyte accumulation at the electrodes thus limiting throughput [12].

Push-pull diffusion involves the pulling of neurochemicals out of the brain from a fluid channel while replacing the extracted fluid volume with saline solution pushed in from another channel [13]. The channels can be formed either with glass capillaries or with microfluidic channels fabricated in either polymers or silicon. The extracted neurochemicals can be then examined using sensitive analytical chemistry methods such as liquid chromatography, capillary electrophoresis, and mass spectrometry [14]-[17]. While push-pull diffusion allows for the detection of multiple neuromodulators simultaneously, it suffers from low sensitivity as all chemicals from the brain are collected thus lowering LODs.

Microdialysis is similar to push-pull diffusion but instead of an open channel at the tip, a thin membrane layer is added at the opening [18]. Fluids, usually saline, are pushed through the channel and neurochemicals are diffused into the fluid as it passes through the membrane area. The membrane increases sensitivity and selectivity compared to push-pull diffusion as the small pores in the membrane filter out large chemicals not involved in neural activities thus allowing only neuromodulators to pass to the fluid for detection. Typical push-pull diffusion and microdialysis methods both suffer from poor temporal resolution (~1 minute) and spatial resolution (>100μm). Invasiveness is also large due to typical probe size approaching several mm [19]. Table 2.1 summarizes the tradeoffs between the four different methods. Capillary approaches are easy and quick to fabricate but suffer from spatial resolution and are very invasive to the brain while silicon-based approaches are more intensive to develop and fabricate but increase spatial resolution and reduce damage to the brain.

Table 2.1: Fundamental tradeoffs of optical, electrochemical, push-pull and microdialysis neurochemical sensing methods.

Method	**Spatial Resolution**	**Temporal Resolution**	**Chemical Resolution**	**Selectivity**	**Invasiveness**
Optical	Good	Good	Good	Limited	None
Electrochemical	Good	Good	Poor	Limited	High
Push-Pull	Poor	Poor	Poor	Good	High
Microdialysis	Poor	Poor	Good	Good	High

Microdialysis has proven to be the preferred method to sample analytes from the ECS during brain activities due to its high selectivity and sensitivity yielding attomole LODs. Microdialysis is therefore chosen as the base method for the development presented in this work.

In order to accomplish the goals of this project, poor spatial and temporal resolution must be addressed. Spatial resolution can be improved by minimizing the size of neuroprobe with microfluidic channels to the order of 10μm, which are unprecedented in neuroprobes, using modern silicon processing technologies. Reducing the size of the probe also limits damage to the brain that might affect collection of useful information for the black box model. Temporal resolution, on the other hand, is heavily affected by Taylor shear-induced dispersion in long microfluidic channels that smears the concentration distribution in the direction of the flow. This smearing enlarges the area in which collected analytes occupy thus reducing temporal resolution.

Taylor dispersion occurs in fluidic channels due to the creation of two concentration gradients caused by the parabolic flow profile during laminar flow. As the analyte flows into the channel, fluids near the boundaries of the channel will experience higher hydrodynamic resistance due to fluid's tendency to stick to walls. These boundary conditions lead to the flow rate at the center of the channel being higher than that at the sidewalls hence the parabolic flow profile. This protrusion causes the concentration of the analytes at the center of the channel being greater than that at the sidewalls at the same longitudinal position thereby creating a concentration gradient in the latitudinal direction. Analytes from the tip of the protrusion will diffuse down this gradient in order to reestablish equilibrium thereby smearing the signal. At the same time, a concentration gradient is also formed at the back of the flow profile due to the slower flow rates at the side walls. Analytes will likewise move down this concentration gradient at the back to reestablish equilibrium. The result is the enlargement of the signal area thereby degrading temporal resolution. As analytes must travel relatively long distances from the brain to the detection area, effects of Taylor dispersion are compounded thereby leading to significant loss of temporal resolution. Figure 2.1 graphically shows the mechanisms of Taylor dispersion.

To improve temporal resolution in microdialysis probes as desired, it is imperative to limit the effects of Taylor dispersion. One effective way to accomplish this is to trap the collected neurochemicals in droplets. As the analytes are encapsulated, the concentration within each droplet remains constant as it travels over long channels thus eliminating Taylor dispersion. It has been proven that encapsulating the analytes in droplets at the base of a probe can lower

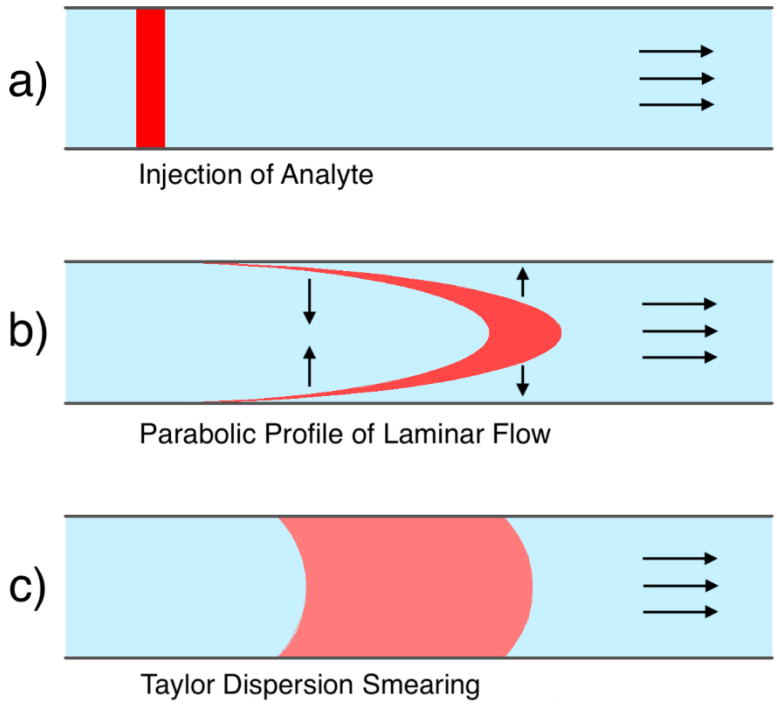

Figure 2.1: Schematic describing Taylor dispersion mechanism. a) Injection of analyte into fluid stream. b) Laminar flow causes parabolic flow profile of analyte creating two concentration gradients at the head and tail. c) Analyte moves down the chemical gradient to reestablish equilibrium thus smearing analyte.

temporal resolution in microdialysis probes to 6 seconds [20]. As the droplets are generated at the base of the probe, significant Taylor dispersion still occurs at the length between the sampling area and the base of the probe which can be several millimeters long. Temporal resolution can therefore be improved upon by generating the droplets at the tip of the probe close to the sampling area thus greatly reducing the effect of Taylor dispersion. To this end two types of channel need to be developed. The first are bulk microfluidic channels etched into silicon responsible for transport of fluids between the base of the probe to the tip. Surface microfluidic channels at the tip of the neuroprobe constitute the second and are responsible for droplet generation and diffusion of neurochemical through a porous membrane. By using surface channel structures, the membrane area and the droplet generation structure can be easily fabricated next to each other. Figure 2.2 shows a schematic view of the final proposed structure.

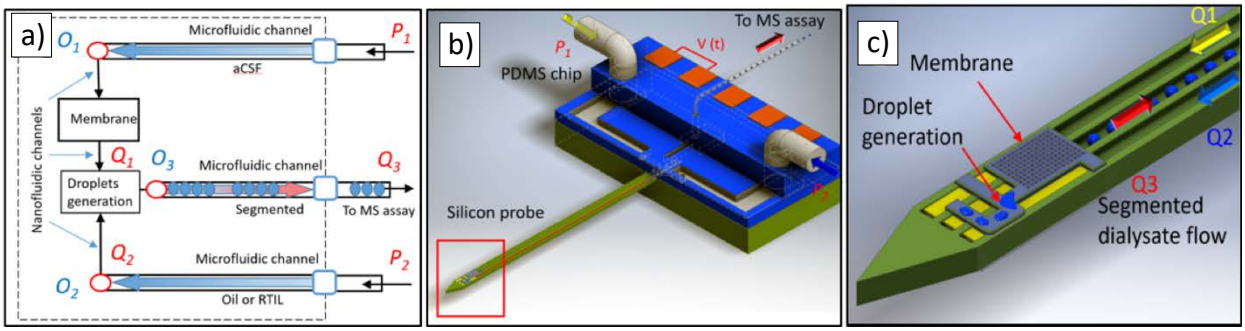

Figure 2.2: Schematic and model of the proposed microdialysis neurochemical probe with droplet generation. Images reprinted from NIH Grant 1UF1NS107677-01. a) Schematic flow diagram of fluid flow within the neuroprobe. Pressure gradient is applied to the inlet channels driving the flow of the fluids. Analyte diffuses through the membrane and is immediately encapsulated with droplets and pushed through to the outlet via a third microfluidic channel. b) High level model of proposed neuroprobe showing the needle and base with inlet and outlet holes. c) Zoomed in view of the tip of the probe. Three bulk silicon channels are etched into the probe. The two on the side push the water and oil phase fluids while the middle channel transfers the droplets to the outlet. Water phase fluid moves from the bulk channel to the membrane area on the surface channels while oil phase flows into the surface channel right after the membrane area to generate droplets after which droplets are pushed down to the middle channel from the surface channels.

Chapter 3: Surface Microchannel Fabrication

3.1: Fabrication Process Overview

Surface microchannels are fabricated using standard silicon fabrication techniques. As these channels are designed to be placed on top of bulk silicon channels that require a layer of oxide on the surface as part of the fabrication process, silicon wafers with pre-grown thermal oxide are used as the substrates.

The overall fabrication process is shown in Figure 3.1. The general method to fabricate the channels is to use negative photoresists as a sacrificial core over which a layer of silicon oxide is deposited. The photoresist core is then finally etched away to create the hollow fluidic channel. Fabrication is fully done in the cleanroom located in the Micro and Nano Technology Laboratory (MNTL) at The University of Illinois at Urbana-Champaign.

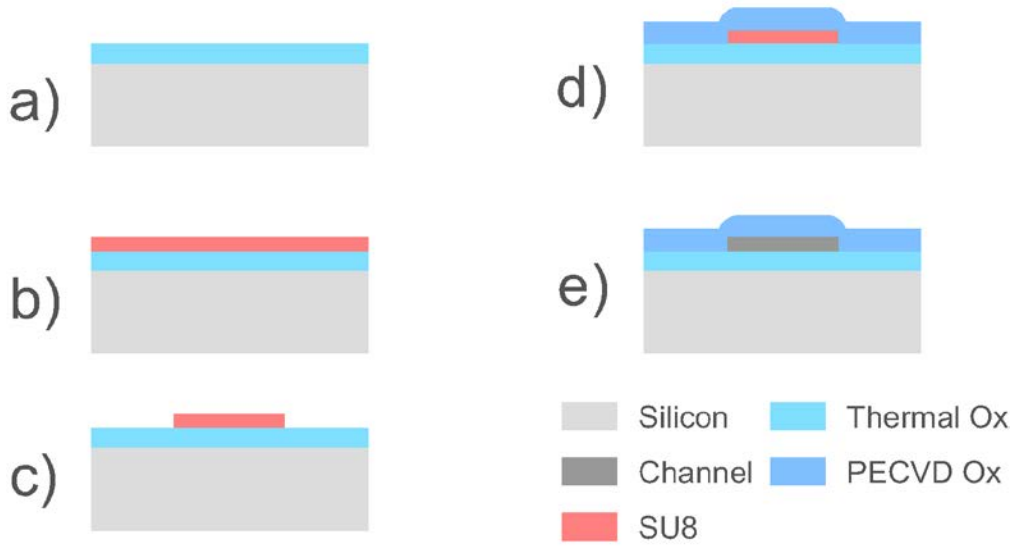

Figure 3.1: Cross-section process schematics for fabrication of surface microchannel. a) Silicon substrate with pre-grown thermal oxide is used as the main substrate for this development. b) A layer of SU8 photoresist is spin coated onto the wafer. c) The SU8 photoresist is exposed and patterned to have the dimensions of the channels. d) A layer of PECVD oxide is deposited on top of the resist. e) The SU8 sacrificial core is etched away using piranha etchant.

A four-inch <100> silicon wafer with 1µm of pre-grown thermal oxide from University Wafers is cleaved into 2cm by 2cm square pieces to form the substrate. Chemically amplified SU8-2000.5 negative photoresist from MicroChem is patterned and used as the sacrificial core.

3.2: Substrate Preparation

The four-inch thermal oxide wafer is cleaved into multiple 2cm by 2cm square pieces by using a diamond scribe. The scribe first indents the surface of the wafer marking the required dimensions and is then cleaved apart using a ridge along the <100> crystalline orientation.

The substrate pieces are then cleaned of organic residues using 3:1 piranha solution for 5 minutes. The piece is then rinsed with deionized (DI) water and air-dried using nitrogen gas followed by a dehydration bake at 110˚C for 5 minutes. The 3:1 piranha solution is made of 3 parts concentrated sulfuric acid (H_2SO_4) and 1 part 30% hydrogen peroxide (H_2O_2).

3.3: Photoresist Application

After cleaning the substrate, place the substrate onto a spin coater and deposit 1mL of SU8-2000.5. Spin coat the substrate using the three-step recipe listed in Table 3.1. The first step spreads the photoresist evenly across the substrate and spins off excess photoresist. The second stage defines the thickness of the resist with respect to the spin speed and the final stage spins off excess resist accumulated at the edge of the substrate to reduce the formation of edge beads. After spin coating, soft bake the substrate for 1 minute at 95˚C and let rest on cooling plate for 2 minutes. This process will result in the structure shown in Figure 3.1 b.

Table 3.1: Three-step spin coating recipe including spin speed, ramp, and duration.

Step	Speed (rpm)	Ramp (rpm/s)	Duration (s)
1	500	100	5
2	2000	300	30
3	6000	6000	2

The resulting photoresist thickness is 700nm as determined from the calibration curve shown in Figure 3.2. The curve is obtained by varying the second step spin speed between 500rpm and 3000rpm while keeping the ramp and duration time constant. For each spin speed, the resulting thickness is measured three times using ellipsometry at a different location and then averaged. It was determined that uneven coating occurs for speed below 600rpm thereby limiting maximum resist thickness to approximately 1µm. It is also observed that the thickness flatlines at 700nm beginning at 2000rpm for this photoresist formulation. As the goal is to minimize the cross-section area of the microfluidic channel, the spin speed at which the flatline thickness is first reached is used for this development.

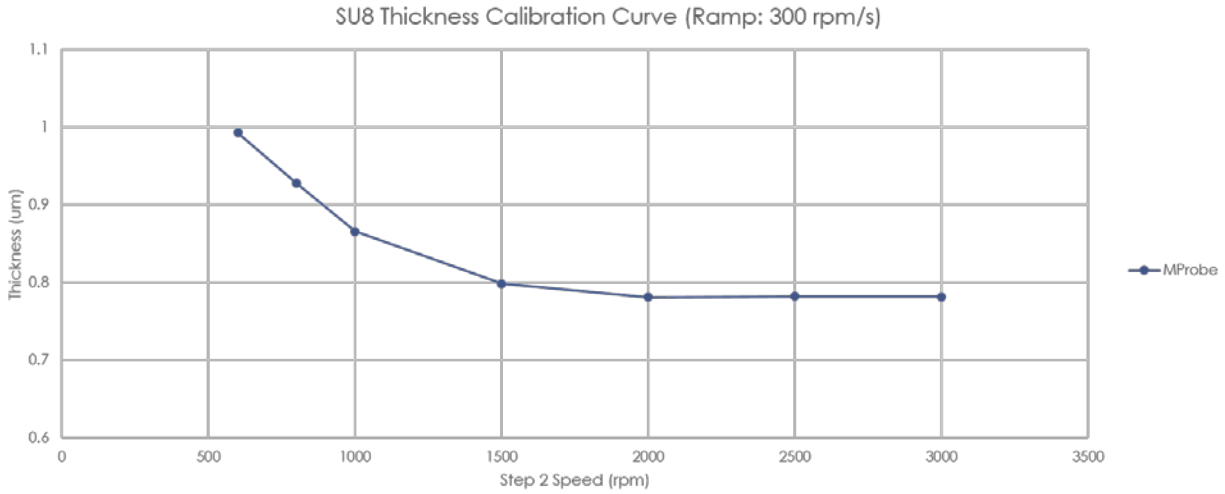

Figure 3.2: SU8 2000.5 spin coating thickness calibration curve. Only speed at the second stage is adjusted while the ramp and duration remained constant.

The Headway Spinner is used to spin coat the photoresist. This spinner, shown in Figure 3.3, is capable of spin coating wafer pieces up to 4-inch whole wafers with spin recipes consisting up to nine speed steps.

Thickness of photoresist is determined via ellipsometry using the MProbe system shown in Figure 3.4. The MProbe measures the change in both amplitude and phase of reflected light beam due to thickness and refractive index of the photoresist and computes the thickness based on known spectrum properties of the photoresist.

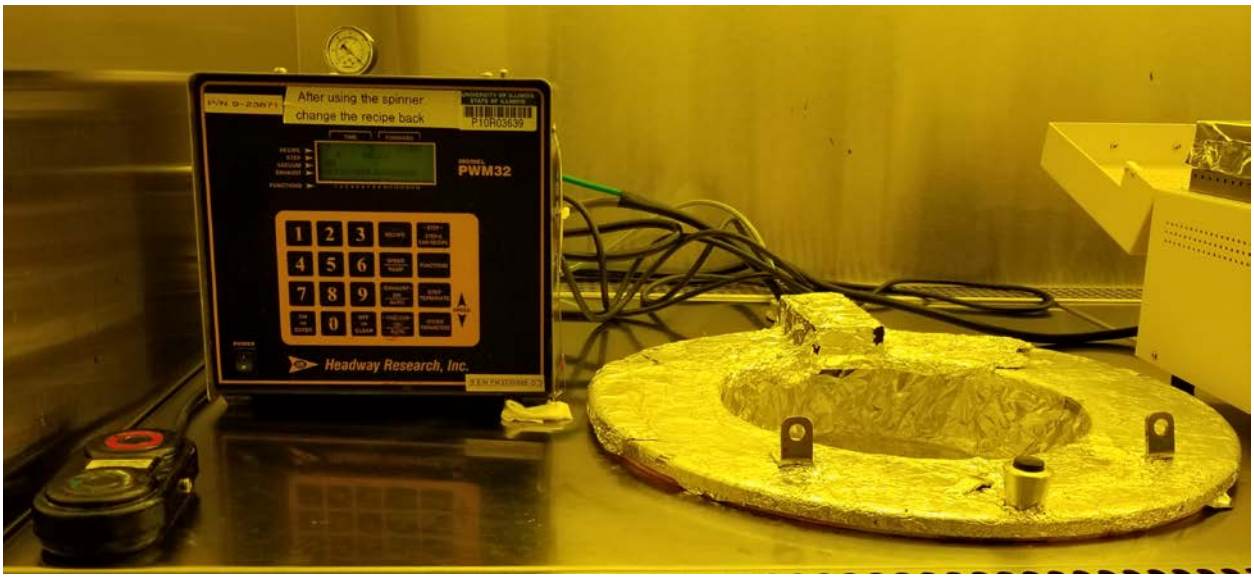

Figure 3.3: Headway Spinner in MNTL. Left box is controller for the spinner. Right side bowl used for spin coating.

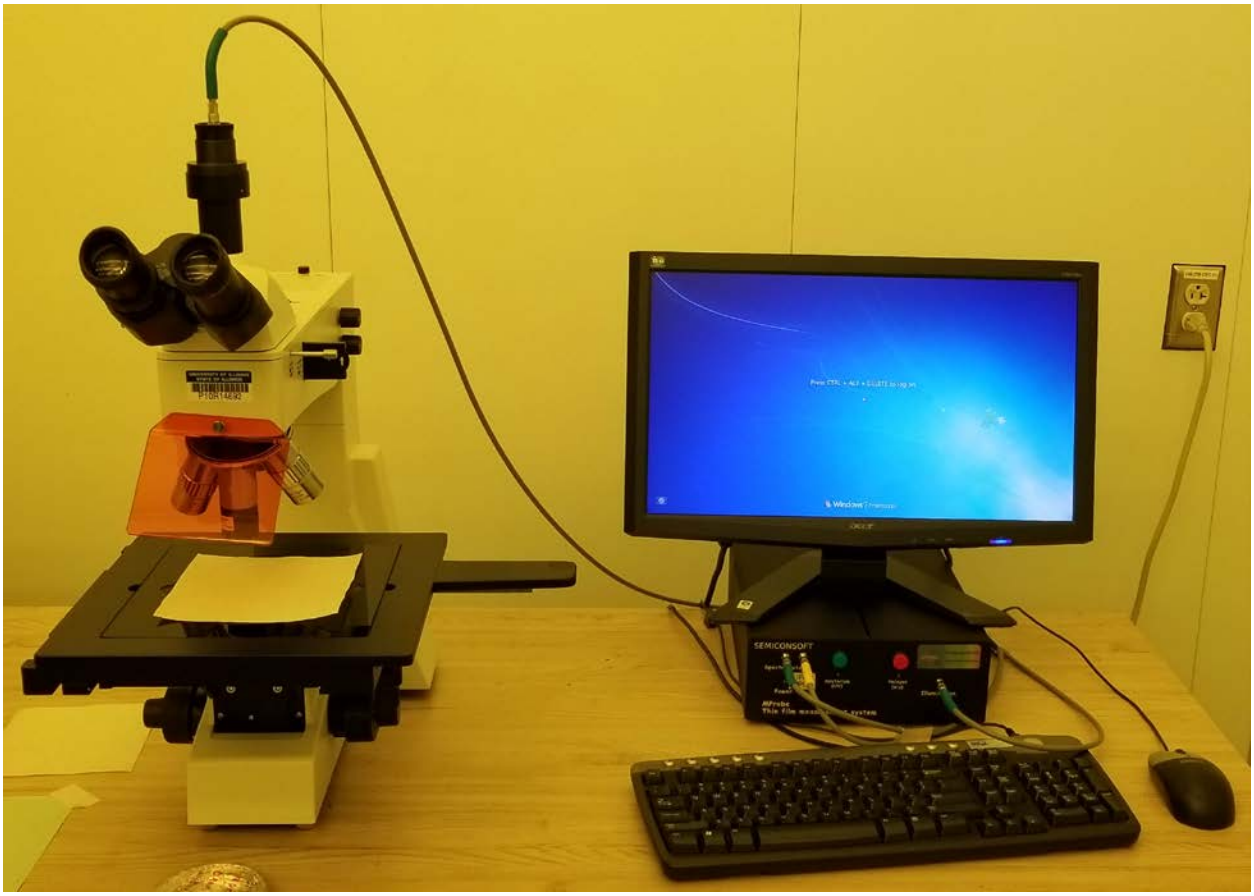

Figure 3.4: MProbe in MNTL used to measure thickness of thin films. The microscope focuses and collects light to and from the sample to measure change in polarity due to thin films.

3.4: Photolithography

The mask features consist of 4mm long rectangles with width varying from 1.2µm to 3.2µm as shown in Figure 3.5. As SU8-2000.5 is a negative photoresist, the exposed area will cross-link the polymers in the resist causing the features from the mask to remain on the substrate after development.

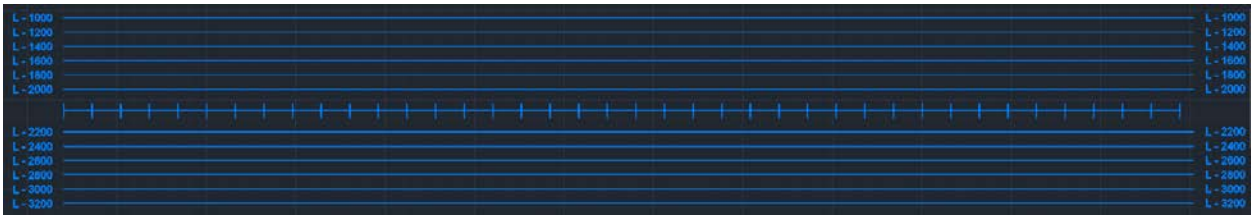

Figure 3.5: Mask features of straight line of width between 1µm and 3.2µm. The feature width defines the width of the resulting microfluidic channel.

After photoresist coating and soft baking, the substrate piece needs to have its edge cleaved off to eliminate edge bead buildup that is shown in Figure 3.6. To prevent silicon debris from being trapped on the photoresist surface, a water-based hydrogel (Aloe Vera) is applied at the edges of the substrate. The debris from the cleaving procedure will be trapped by hydrogel which can be then rinsed off from the substrate using DI water without damaging the photoresist.

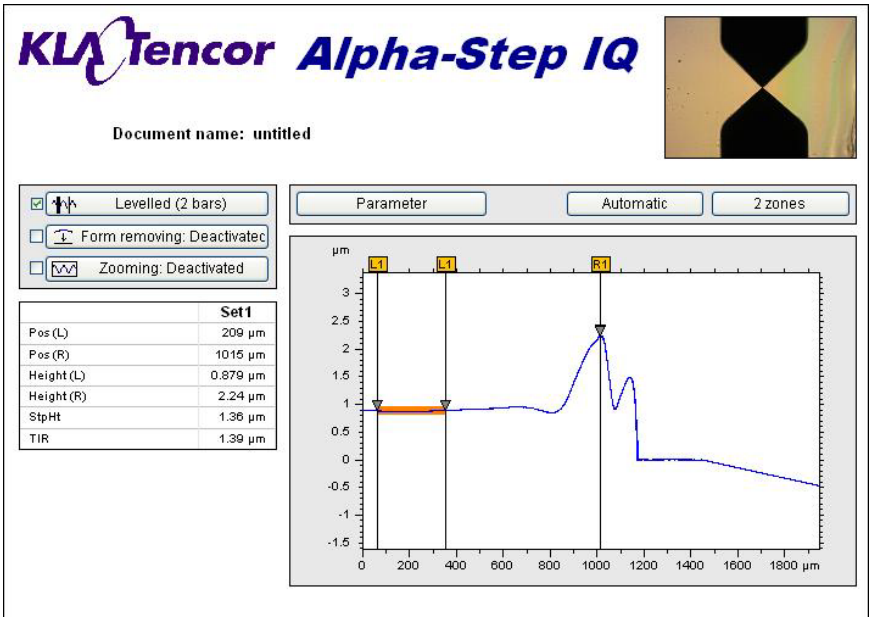

Figure 3.6: Profilometer measurement of the edge bead after spin coating SU8 photoresist. The edge bead builds up to 1.36µm causing air gaps between the substrate and the mask thus degrading lithography resolution.

After rinsing and drying the substrate with nitrogen air, expose the substrate with a contact aligner with a 320nm wavelength light source in vacuum contact mode. The total exposure energy is 54mJ/cm^2. For the post-exposure bake, bake the sample for 5 minutes at 65˚C and then ramp temperature to 95˚C. Let the substrate bake at 95˚C for 1 minute. Let the substrate cool for 1 minute before submerging it for 1 minute in SU8 Developer purchased from MicroChem. Rinse the sample with fresh developer followed by isopropyl alcohol (IPA) and blow drying with nitrogen air. The substrate has cross-section features shown in Figure 3.1 c after this process.

Figure 3.7 shows the experimentally obtained exposure curve from which the final exposure energy is determined. The curve is obtained by varying the exposure energy from 36mJ/cm^2 to 63mJ/cm^2 and measuring the resulting width of the rectangular features, in this case mask feature of width 1.2µm and 3.2µm. The width of the resist features is measured using cross-sectional scanning electron microscope (SEM) images. From the calibration curve, it is seen that the resulting feature width that most closely matches that on the mask occurs with exposure energy of 54mJ/cm^2.

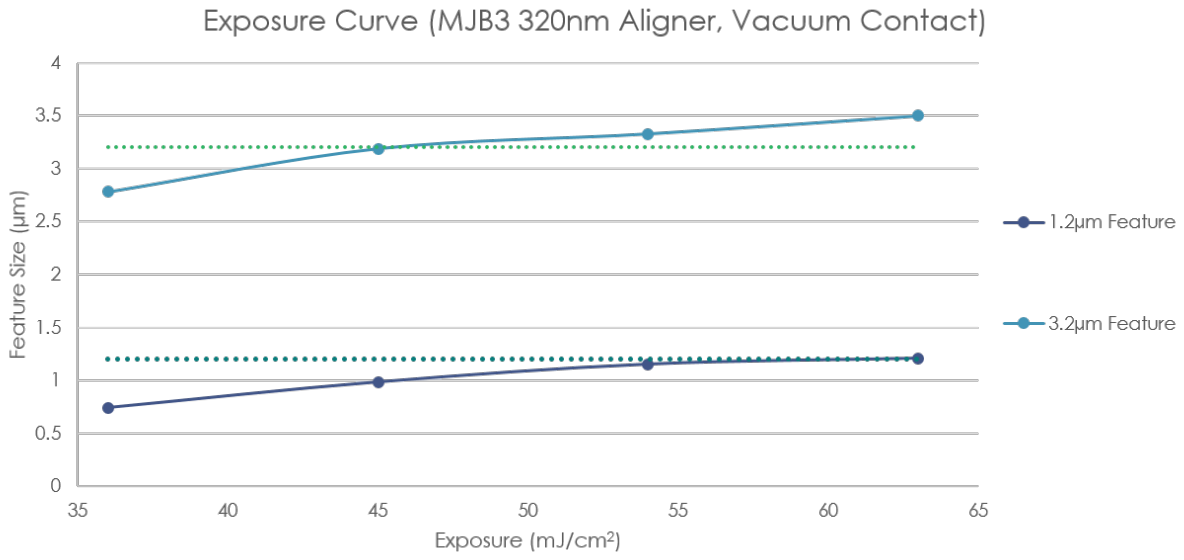

Figure 3.7: Exposure curve of SU8 2000.5 with MJB3 aligner exposing with 320nm wavelength UV light. The dotted line indicates the feature size on the mask.

The Karl Suss – MJB3 A Aligner in the MNTL cleanroom, Figure 3.8, is used to expose the samples. This contact aligner is equipped with a 320nm light source and can take sample size up to 2-inch wafer pieces and 3-inch mask. The aligner is tuned to have power of 9W/cm^2 and can operate in three modes: (1) soft contact where substrate is pushed mechanically toward the mask, (2) hard contact where the air pushes substrate towards the mask, and (3) vacuum contact where a vacuum is pulled between the substrate and the mask.

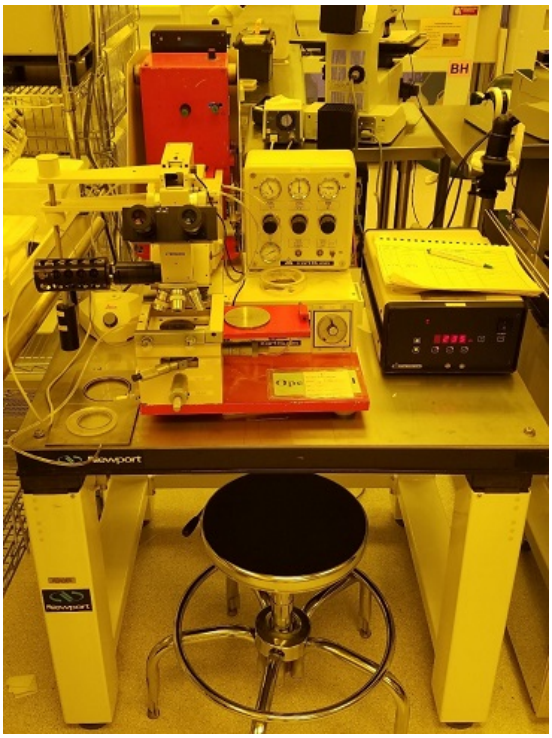

Figure 3.8: Karl Suss MJB3 Mask Aligner. The right box is the power source for the lamp. Alignment is done using the microscope while moving a 3-axis stage. The aligner is best suited for exposure of small sample pieces.

3.5: Oxide Deposition

Following photolithography, oxide is deposited on top of the resist features to create cross-sections shown in Figure 3.1 d. Before deposition of oxide, the resist features need to be hard baked to prevent degassing and reflow in the deposition chamber. For the hard bake, the sample is baked at 65˚C for 5 minutes before ramping the temperature to 260˚C where it will be baked for an additional 10 minutes after reaching 260˚C. Cool the substrate on a cooling block for 10 minutes.

Plasma enhanced chemical vapor deposition (PECVD) is used to deposit silicon oxide as it is a low temperature process. Table 3.2 lists the deposition settings used to achieve a thin film oxide with deposition rate of 340Å/min and conformality ratio of 1.3. The conformality ratio is defined as the ratio of the thickness of the oxide overhanging the photoresist features to that of the sidewalls at an ideally 40˚ angle.

Table 3.2: Three step spin coating recipe including spin speed, ramp, and duration.

Parameters	**Settings**
Platen Temperature	200˚C
Pressure	500mTorr
Power	34.7W
Silane (SiH_4) Gas Flow	3 sccm
Nitrous Oxide (N_2O) Gas Flow	114.24 sccm

The optimal recipe shown in Table 3.2 is determined from calibration curves shown in Figure 3.9 to 3.11. Deposition rate is obtained by taking the difference of oxide thickness before and after PECVD and dividing it over the total deposition time. The thickness is measured using the MProbe mentioned in Section 3.3. The conformality ratio is obtained by measuring the respective thickness of the oxide using a cross-section SEM image such as that shown in Figure 3.12.

The PECVD is done using the Plasmalab PECVD tool, Figure 3.13, in the MNTL cleanroom. This tool allows for the deposition of silicon oxide at low temperatures making it compatible with SU8 photoresists. The system uses a 13.56MHz RF power supply. The silane gas used by the tool has a 5% N_2O buffer. The tool takes input of power in percentages of max power provided by the supply and gas flow in percentages of the gas flow controller. For the optimal recipe, the equivalent percentage parameter value for power is 13.4%, silane gas flow is 60%, and N_2O gas flow is 80%. The tool requires chamber cleaning with chloride gas after every micron of deposition to maintain uniform deposited oxide film.

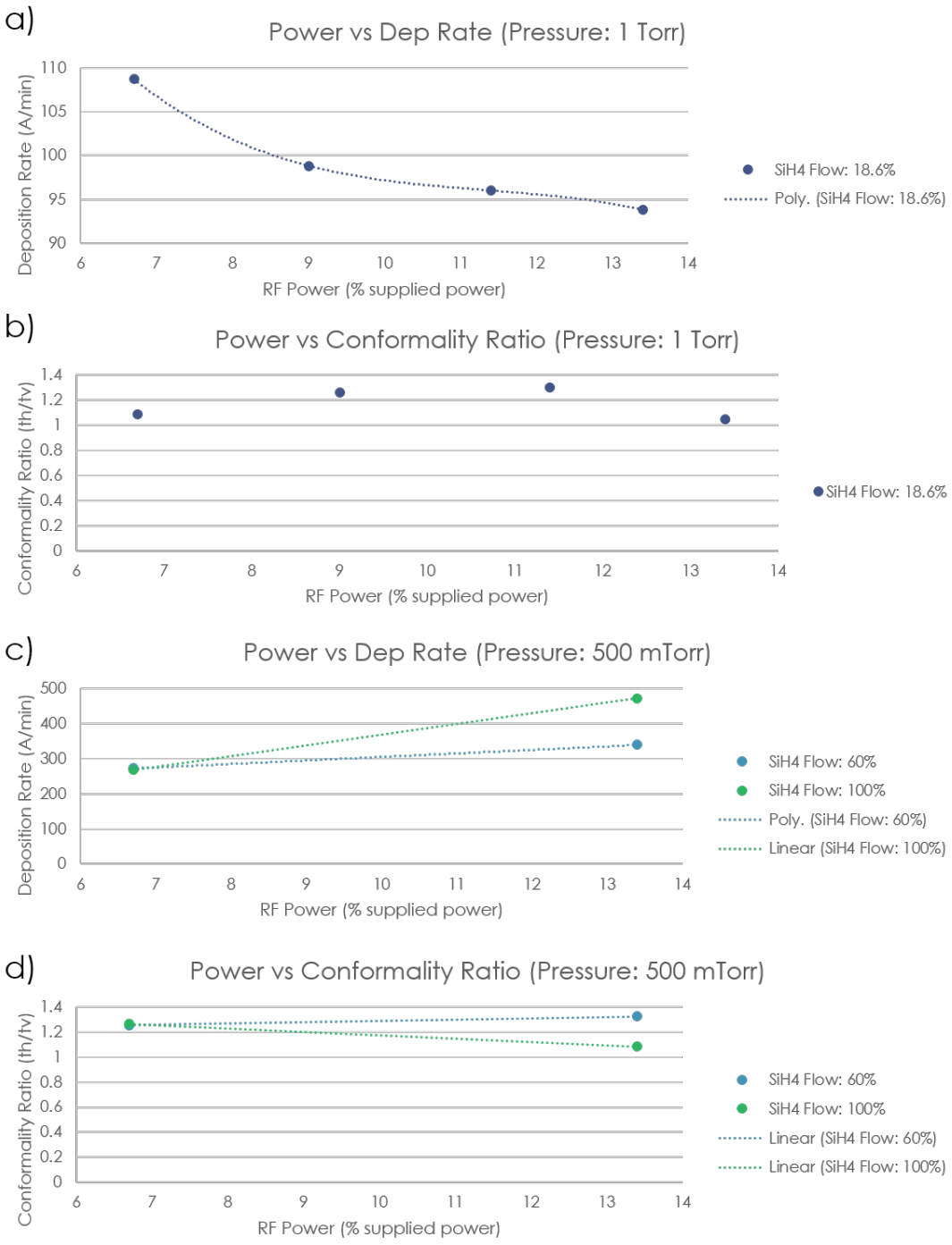

Figure 3.9: Calibration curves of PECVD with regards to supplied power. a) Deposition rate decreases with increase in power at high pressure. b) The conformality of the film is relatively constant with change in power under high pressure conditions. c) As expected, the deposition rate under low pressure increases with increase in power. d) Likewise, the conformality is consistent with change in amount of power being supplied under low pressure conditions.

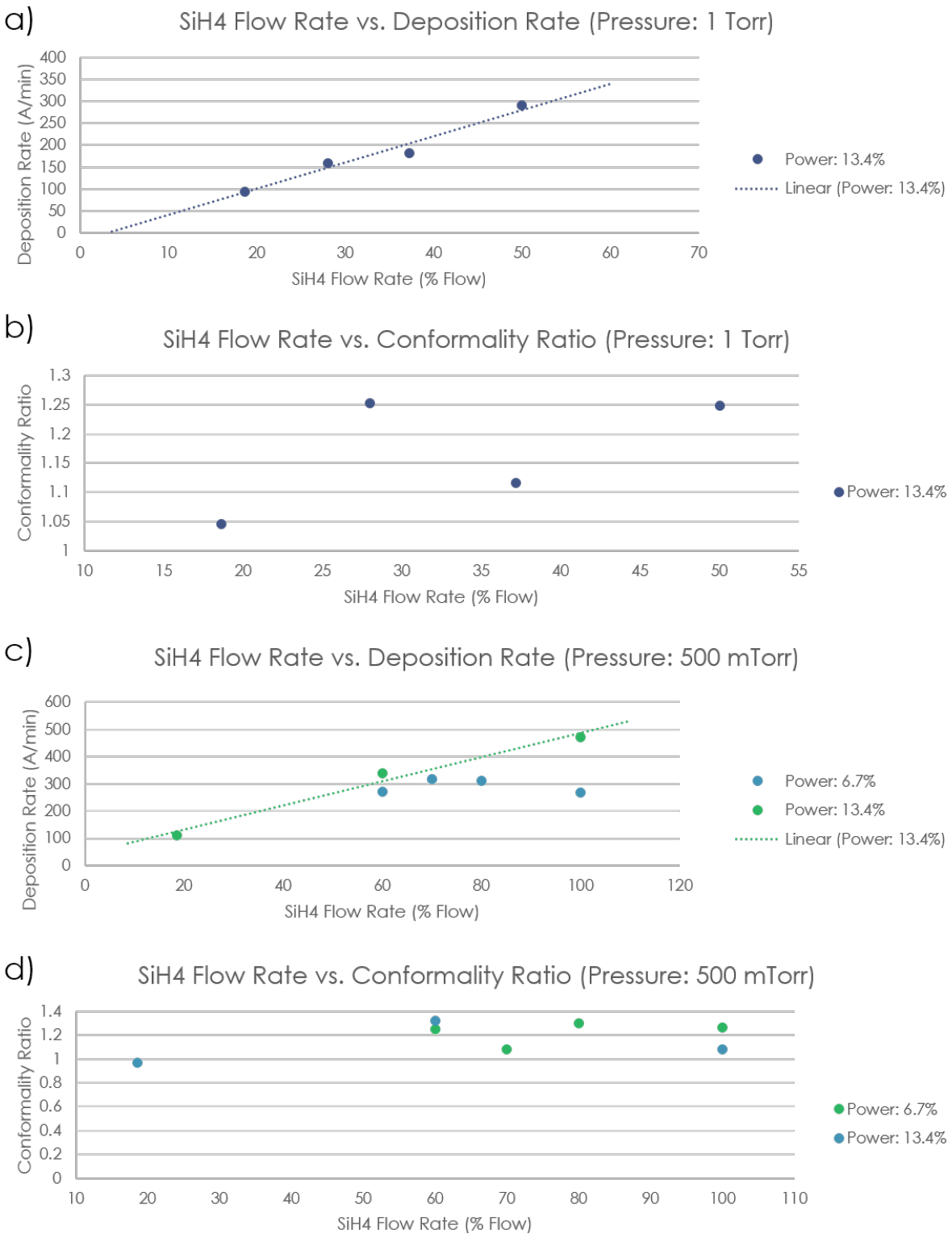

Figure 3.10: Calibration curves of PECVD with regards to silane gas flow. a) Deposition rate increase with increase in silane gas flow as expected. b) The conformality of the film is relatively constant with change in gas flow. c) As expected, the deposition rate also increases with increase in silane gas flow. d) Likewise, the conformality is consistent with change in amount of silane being supplied under low pressure conditions.

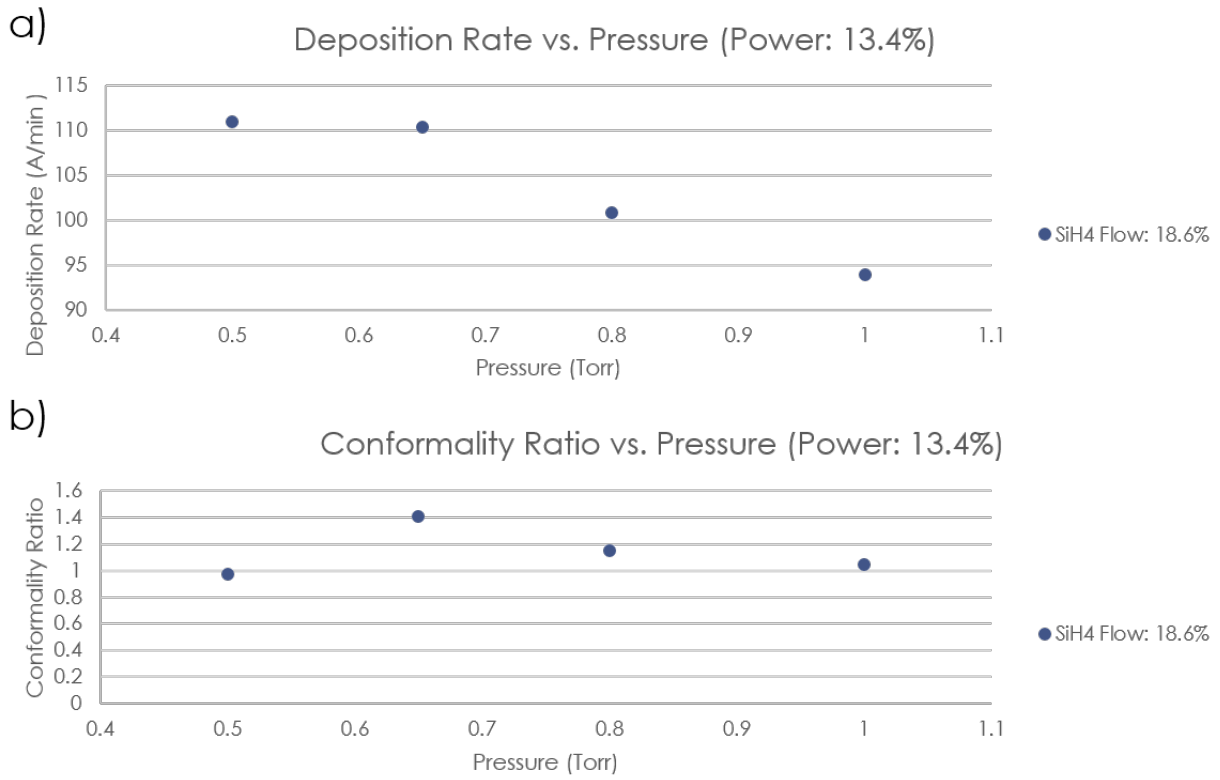

Figure 3.11: Calibration curves of PECVD with regards to chamber pressure. a) Deposition rate increased with higher chamber pressure as was expected. b) The conformality of the film is relatively constant with change in pressure.

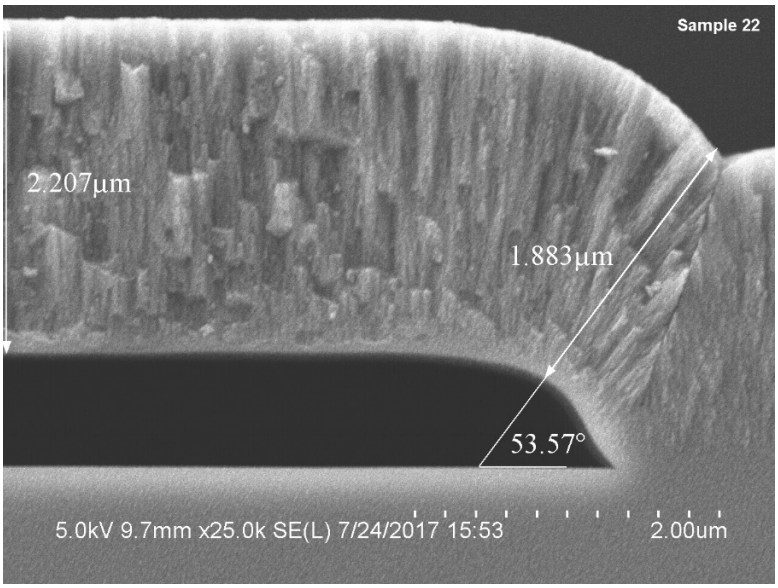

Figure 3.12: A sample cross-section SEM image used to calculate deposition rate and conformality issue. Deposition rate is taken as the amount of oxide deposited on top of the photoresist and dividing it over the total deposition time. Conformality is measured at a known angle, which in this case is 53.37 degrees. The ratio is of the thickness on the top to that on the side at the set angle.

3.6: Sacrificial Core Removal

To achieve the hollow microfluidic channel as shown in Figure 3.1 e, the SU8 photoresist core needs to be etched away. As the photoresist has been heavily cross-linked due to the hard bake and the PECVD process, it can only be removed using an aggressive 1:1 piranha etch solution. To begin etching the channel, first expose the core by cleaving one or both ends of the channel. Submerge the wafer in one part sulfuric acid (H_2SO_4) and one part 30% hydrogen peroxide (H_2O_2) to create the 1:1 piranha solution. Place the bath with the sample on a hotplate set to 100˚C and cover it to prevent evaporation. As 1:1 piranha solution is extremely flammable, do this process with the utmost care. When the desired etch time is reached, remove the substrate from the bath and quench and rinse with DI water follow by blow drying with nitrogen gas.

Etching rate is dependent on the cross-section dimension of the channels and the amount of deposited PECVD oxide. Figure 3.13 shows graphs of extracted etching rate from various channel dimensions and total etching time as well as amount of deposited PECVD oxide. The total etch distance used to obtain the etch rate is measured via an optical image such as that shown in Figure 3.14. The etch distance can be determined by totaling the pixels across the length and relating that number to the total pixels covering the width of known channels.

Pressure buildup occurs in the channel during etching of the core as reactants and products from the etch are trapped within the channel that can lead to channel breakage. The survivability of the channel is closely related to its width and oxide thickness [21]. As the width of the channel increases, it becomes more prone to breakage while with increased oxide thickness, the channel is better able to withstand pressure buildup and thus less prone to breakage. Figure 3.15 shows tabulated results of survivability of channels in terms of minimum width at which breakage of the channels can be observed against the deposited oxide film thickness.

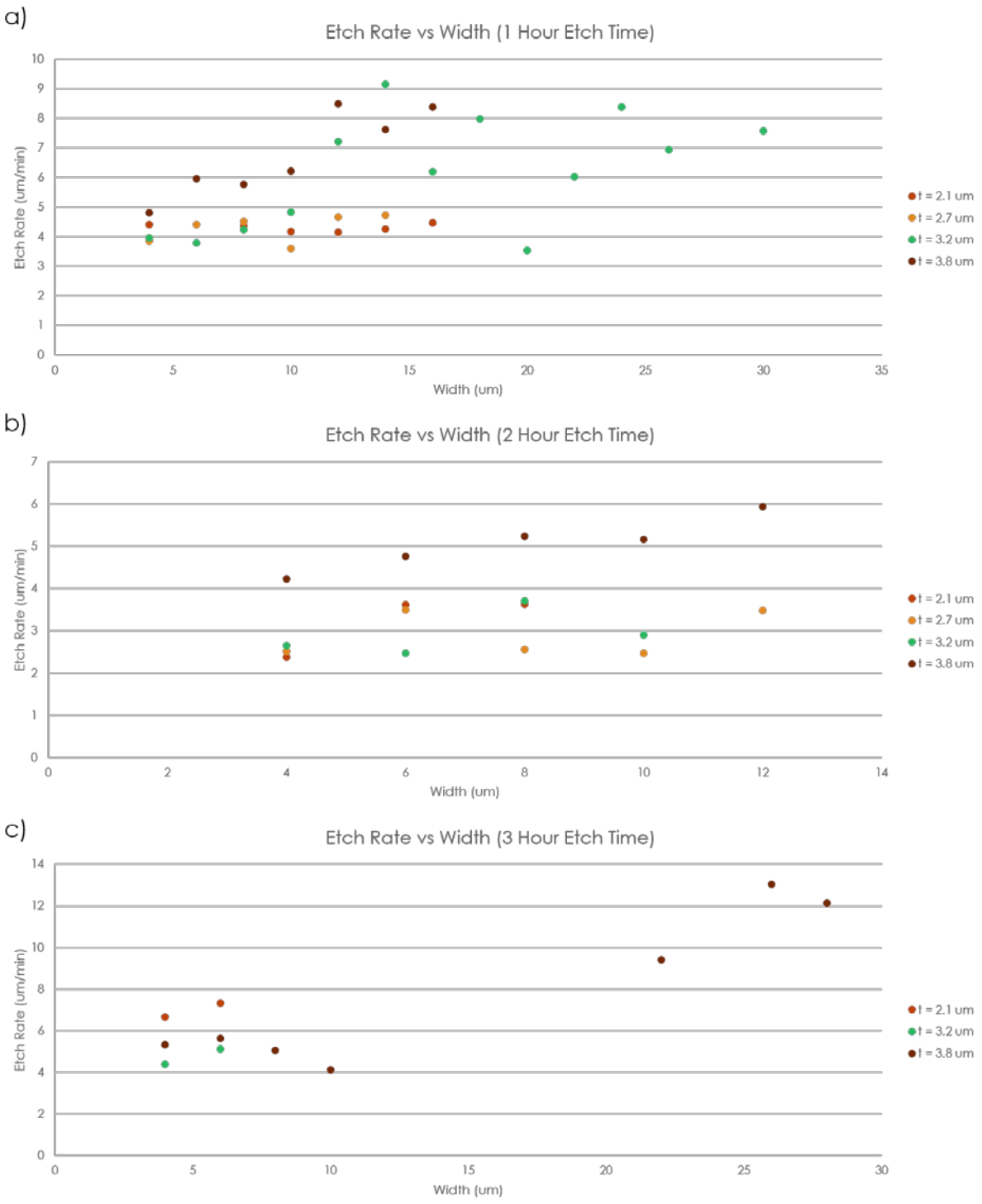

Figure 3.13: SU8 etch rate within microfluidic channel. Etch rate measured as the amount of material removed along the channel over the total etch time during which samples are in Piranha etching solution. a) Etch rate determined from samples in Piranha etch for 1 hour. b) Etch rate determined from samples in Piranha etch for 2 hours. c) Etch rate determined from samples in Piranha etch for 3 hours. From the three graphs, it seems that the width of the channel does not play an important part in the etching speed as most data points for a single oxide thickness are relatively flat. However, the thickness of oxide seems to affect the etch rate positively as the thicker oxide is etched out of the channel.

Figure 3.14: Microfluidic channel with SU8 core partially etched away. The channels have two different colorations with the lighter area indicating hollow channels and the darker area indicating channels with SU8 presence. These channels are intact as no observable cracks can be seen from the substrate surface.

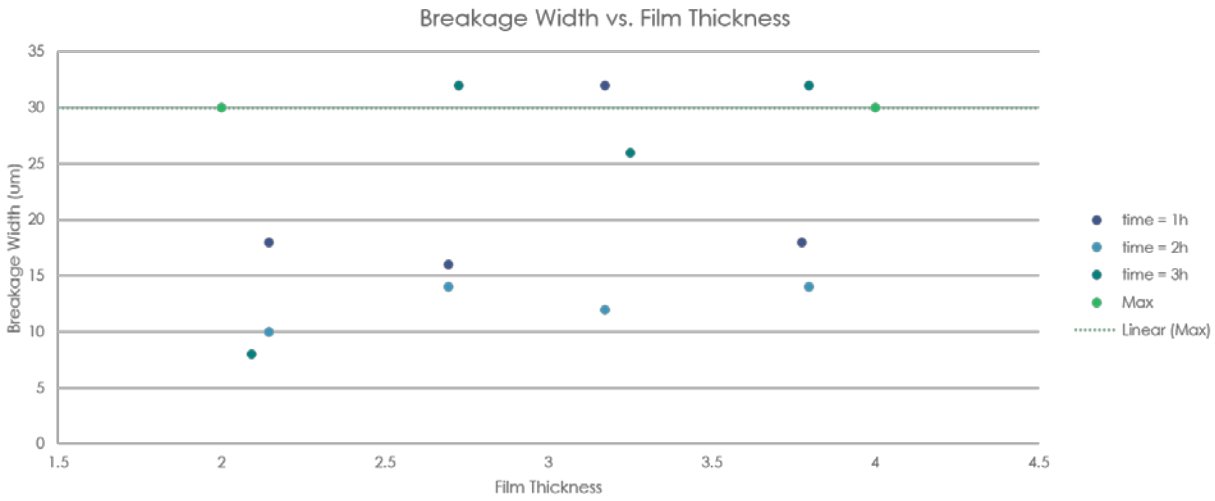

Figure 3.15: This graph shows for what oxide thickness and channel width the channel will start to form cracks and break. Based on the values presented in this graph, it can be deduced that channels can go up to 10µm in width before breakage starts to occur and that film thickness above 2.5µm does not aid in the integrity of the channel.

Chapter 4: Neuroprobe Fabrication

4.1: Neuroprobe Fabrication Overview

The neuroprobes are fabricated on silicon-on-insulator (SOI) wafers purchased from Ultrasil with the following dimensions: 500µm handle side silicon, 1µm buried oxide (BOx), and 15µm device side silicon.

The resulting neuroprobes consist of a 2mm by 2mm base of the same thickness as the SOI substrate, namely 516µm, and a needle with the same thickness as the device-side silicon, namely 15µm, and width of 75µm at the base and 55µm at the tip. Figure 4.1 shows the top-level schematic fabrication flow for the neuroprobe.

The probe consists of two bulk silicon microfluidic channels etched into the device-side silicon. These channels are designed and fabricated by fellow graduate student Ari Esters in the Integrated Neuro Technologies lab at the University of Illinois at Urbana-Champaign. A brief overview of the fabrication process for the bulk silicon channel is shown in Figure 4.2.

The silicon neuroprobes are fabricated at the Mirco-Nano Mechanical Systems (MNMS) Cleanroom in the Mechanical Engineering Building at the University of Illinois at Urbana-Champaign. MNMS provides positive SPR220 and negative KMPR 10 photoresist used in photolithography and its respective developer and stripper. Crystal bond used to adhere substrate to carrier wafers is also provided by MNMS. LOR-10A lift-off resist is purchased from MicroChem.

4.2: Plumbing Structure Fabrication

4.2.1: Process Overview

The plumbing system for the neuroprobes is to insert glass capillaries with outer diameter of 360µm and inner diameter of 250µm from the back side of the probe to the channels in the device side at the base of the probe. Specific plumbing and packaging process will be discussed in Chapter 5. This process will thus require holes of at least 360µm in diameter to be etched through the handle-side silicon, buried oxide, and device-side silicon from the handle side of the substrate. Figure 4.3 illustrates the processing steps for plumbing structure fabrication.

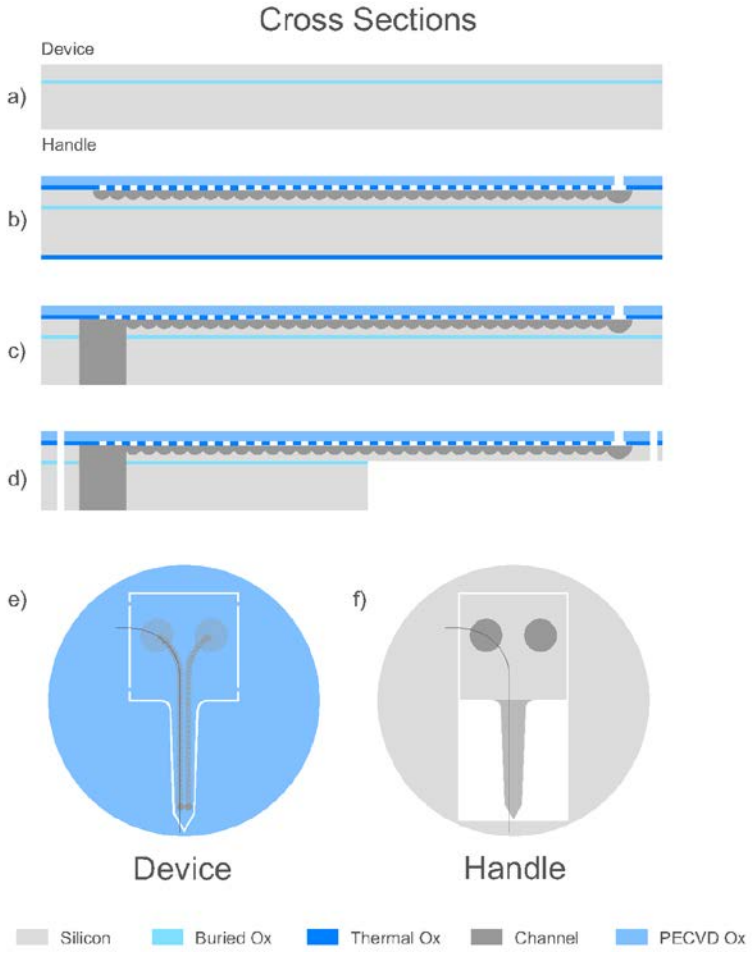

Figure 4.1: a) SOI wafer used to fabricate the neuroprobes. b) Bulk silicon channel fabricated into the device-side silicon of the SOI. c) Plumbing structure etched from the handle side all the way to the channel. d) The probe shape is etched into the SOI wafer creating the released neuroprobes. e) Top view of the device side of the SOI after processing. Note the four silicon bridges holding the probe to the wafer. The line is the cross-section that is shown in a – d. f) Top view of the handle side of the SOI after processing. The line is the cross-section that is shown in a – d.

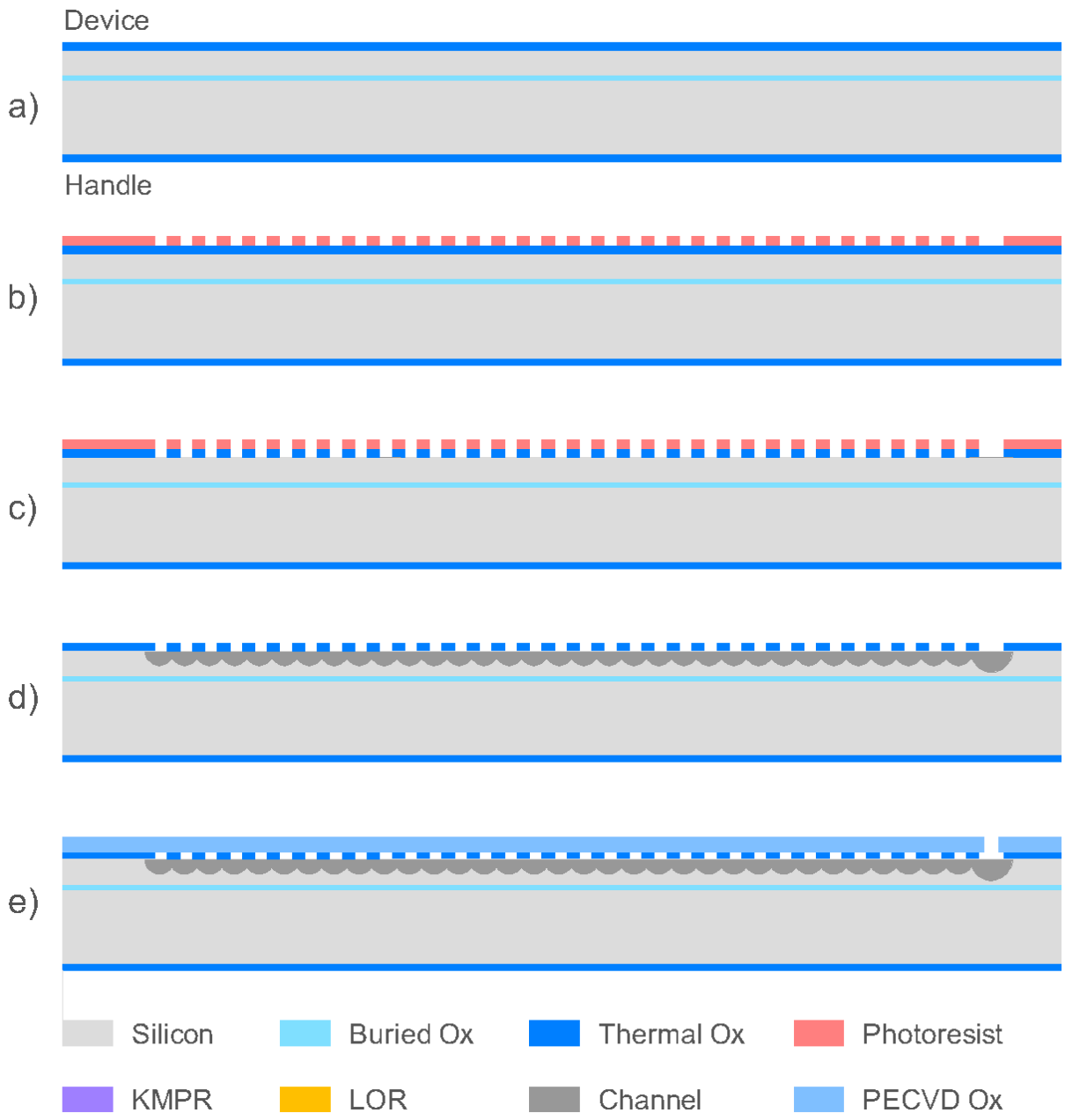

Figure 4.2: Cross-section schematics of bulk silicon channel fabrication. a) Thermal oxide of 150nm is grown on the SOI wafer. b) Photoresist patterned to form array of square features. c) Photoresist features transferred to the thermal oxide to form a hard mask. d) Silicon is isotropically etched with XeF_2 gas after photoresist is stripped off. The resulting semicircular etched features from each square hole will intersect to form the bulk silicon channel. e) The channel is sealed off with a layer of deposit oxide such as PECVD.

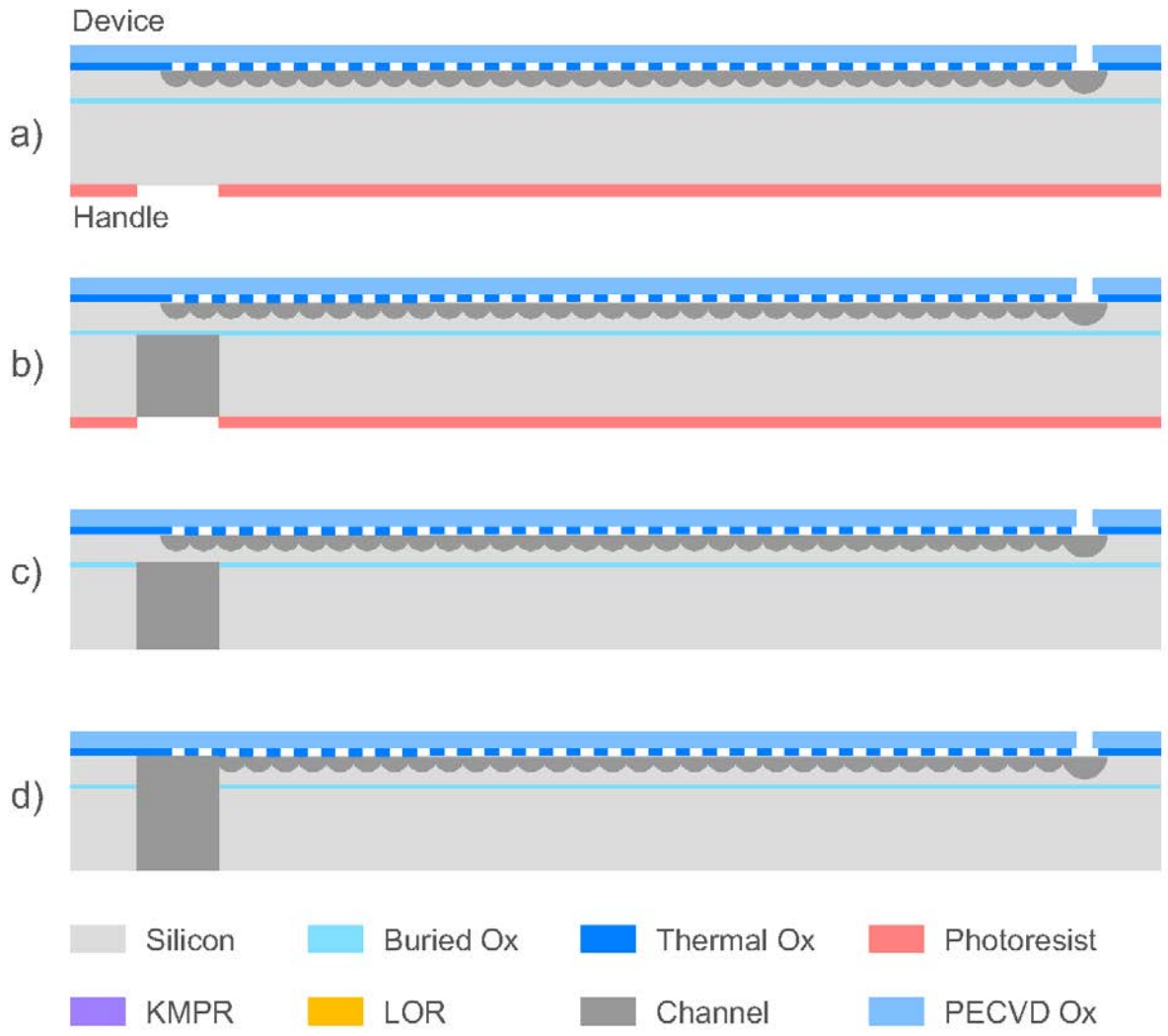

Figure 4.3: Cross-section schematics for plumbing structure fabrication. a) Photoresist spin coated and patterned onto the handle side of wafer to define plumbing hole location and area. b) DRIE is performed to etch away handle-side silicon to the BOx. c) Photoresist is stripped off the wafer before etching away the BOx with ICP RIE. The resist must be stripped before the ICP RIE etch as undergoing both DRIE and ICP RIE will result in the resist hardening to the point where it cannot be stripped off the wafer. d) Device-side silicon between the BOx layer and the channel is etched away to break through the plumbing structure to the channel.

4.2.2: Substrate Preparation

Silicon oxide deposited during channel fabrication on the handle side of the wafer must first be etched away using inductively coupled reactive ion etching (ICP RIE). Etch duration is dependent on whether low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD) is used to seal channels during channel fabrication. LPCVD method requires longer etching time due to oxide being deposited on the handle side of the substrate in addition to the existing thermal oxide from initial wafer oxidation.

The substrate is degreased by spraying acetone, IPA, DI water, and IPA in that order followed by air drying using nitrogen gas. The handle side silicon is then descummed using oxygen plasma reactive ion etching process which will remove any remaining organic residue from the wafer surface. The descummer is set to etch for 1 minute with 100W power and 2:1 oxygen and argon gas mix.

The March Jupiter RIE III, Figure 4.4, in MNMS is used for descumming. The tool is equipped with a 13.56 MHz RF power supply with power output up to 300W. The tool is capable of handling wafers up to four inches and is equipped with both oxygen and argon gas.

Figure 4.4: The March Jupiter III oxygen plasma reactive ion etcher in MNMS used for descumming. The top module is the reaction chamber and the black box on the bottom is the RF power supply.

4.2.3: Lithography

The mask features used in this lithography step consists of a pair of circles with diameter of 400µm for each probe. The circles define the holes used to insert the 360µm diameter capillaries. The features align to the base area of the probe, whose center corresponds to the end of the channels at the base as shown in Figure 4.5.

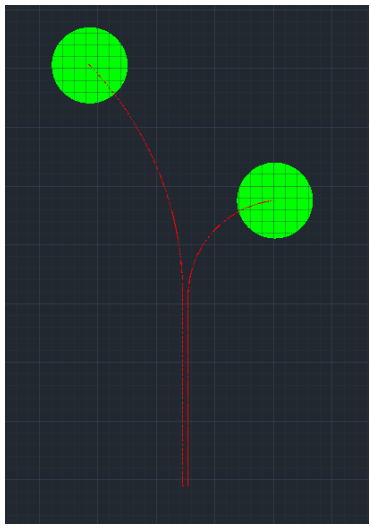

Figure 4.5: The green circles are the mask features used in this process. The red lines are features used in channel fabrication. The center of each plumbing hole is aligned to the end of the channel at the base side (top).

To perform this lithography step, 3.5mL of SPR220 photoresist is first spin coated onto the handle side of the SOI wafer using the three-step spin coat recipe described in Table 4.1. Soft bake the substrate for 1 minute at 110˚C after spin coating. Bottom side alignment is then done to align the plumbing hole structure with the end of the channels at the base. The SPR220 photoresist is exposed with energy of 200mJ/cm^2 using contact lithography in hard contact mode. The resist is developed for 1 minute in Developer AZ 917 MIF to obtain the features shown in Figure 4.3 a. Quench the substrate in DI water for 1 minute after removal from the developer and air dry with nitrogen gas.

Table 4.1: Three-step spin coating recipe including spin speed, ramp, and duration.

Step	Speed (rpm)	Ramp (rpm/s)	Duration (s)
1	500	250	2
2	1500	500	2
3	3000	750	30

The spinner used in MNMS, Figure 4.6, is capable of spin coating wafers up to four inches. The spinner can set up to three spin steps with input of spin speed, acceleration time, and spin duration.

Figure 4.7 shows the EV620 contact aligner used in MNMS. The aligner is equipped with i-line (365nm wavelength) exposure light and can handle wafers up to four inches and masks up to five inches. The aligner is able to do both top-side and bottom-side alignment. For the bottom-side alignment, digital cross-hairs are superimposed on the digital display of the aligner. To align the mask with features on the bottom side of the wafer, the cross-hairs have to be first aligned with alignment marks on the mask before substrate is placed into the system. The alignment marks on the bottom side of substrate are then aligned with the cross-hairs to accomplish the alignment process. Figure 4.8 shows alignment marks both on the mask and the bottom-side substrate for bottom-side alignment.

Figure 4.6: High-speed spin coater in MNMS.

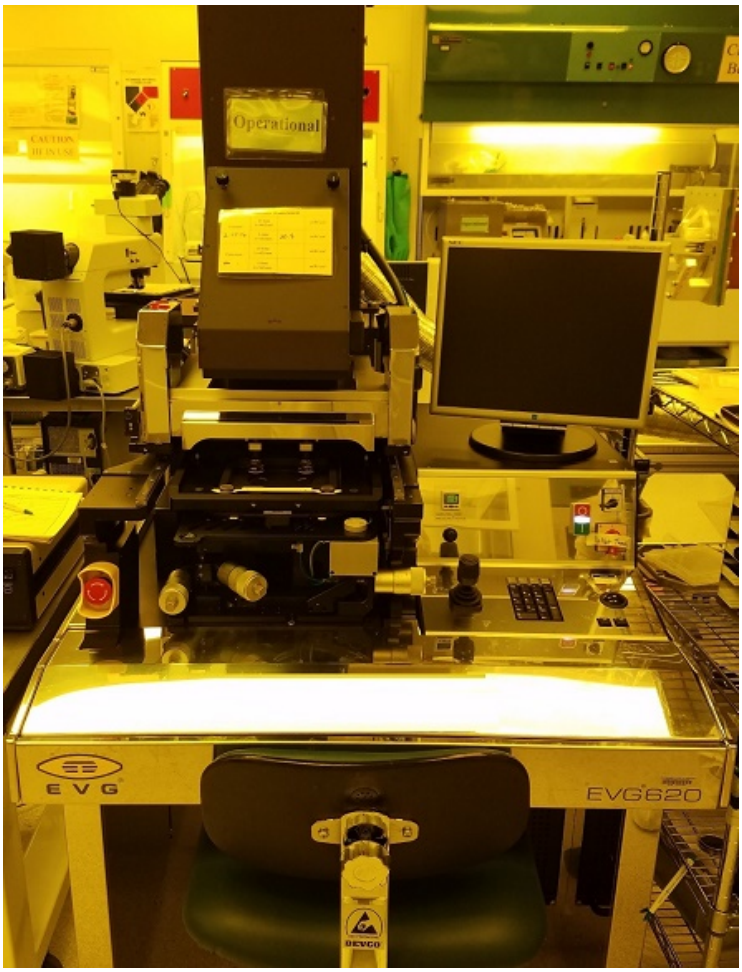

Figure 4.7: EV620 Aligner in MNMS. The top part is the location of the lamp. Alignment is done with the three-axis stage while the microscope and operation are controlled by the accompanying computer program.

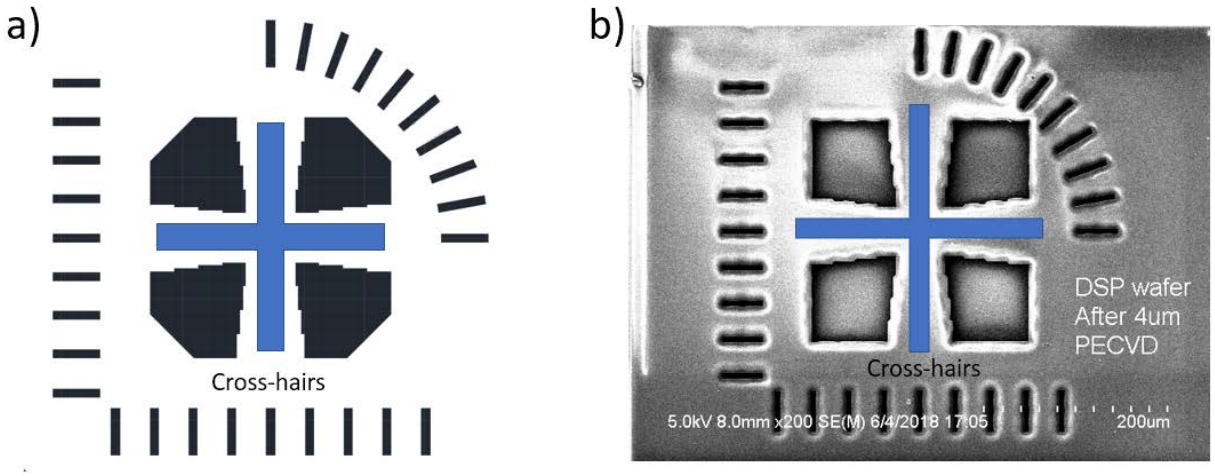

Figure 4.8: Bottom-side alignment marks. The blue cross is the superimposed cross-hairs. a) Digital cross-hairs need to be first aligned to the alignment marks on the mask. b) The cross-hairs then need to be aligned to the mark on the bottom side of the substrate to align the mask to the substrate.

4.2.4: Etching of Plumbing Structure

A three-step etching process is required to fabricate the plumbing structure. The first step, Figure 4.3 b, involves a deep reactive ion etching using the Bosch Process from the handle side of the SOI wafer with the patterned photoresist. This process uses a high-frequency etching recipe that is described in Table 4.2. To etch all the way through the handle-side silicon to the buried oxide layer (BOx), a total of 256 cycles of passivation and etching, or 28.6 total minutes, is needed. Figure 4.9 shows a cross-section image of the plumbing holes after undergoing such DRIE process. Strip the SPR220 photoresist with Microposit Remover 1165 photoresist stripper at 80˚C for 5 minutes or until most of the resist is stripped away. Submerge the substrate stack in a second bath of fresh stripper at 80˚C for an additional 5 minutes to clean off any residue resist.

Table 4.2: DRIE high-frequency (HF) etching recipe.

Parameters	**Settings**
Pressure (Passivation/Etching)	25mTorr/140mTorr
SF_6 Gas Flow (Passivation/Etching)	0sccm/470sccm
C_4F_8 Gas Flow (Passivation/Etching)	200sccm/0sccm
O_2 Gas Flow (Passivation/Etching)	0sccm/45sccm
Passivation Duration per Cycle	4s
Etching Duration per Cycle	7s
Coil Power at 13.56MHz (Passivation/Etching)	2000W/2800W
Platen Power at 13.56MHz (Passivation/Etching)	0W/42W
Temperature	120˚C

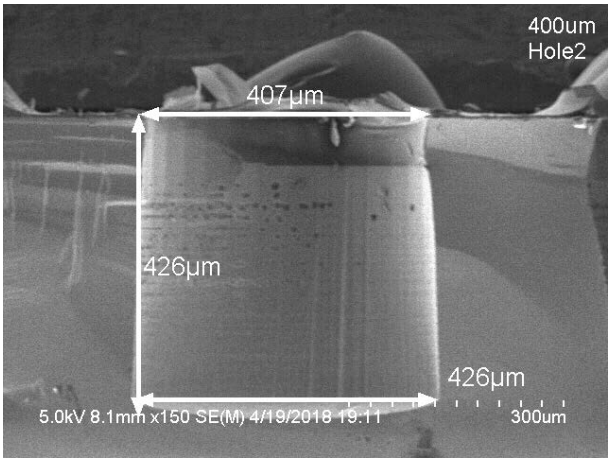

Figure 4.9: Cross-section SEM image of plumbing holes etched into silicon using DRIE. The sample did not etch to the required 500µm as the image is from a 500µm thick silicon wafer.

The exposed BOx is then etched away, Figure 4.3 c, using ICP RIE for 7.5 minutes using the recipe described in Table 4.3. Finally, the thin layer of device silicon between the BOx and the channel needs to be etched away with DRIE, Figure 4.3E. This is performed using a low-frequency (LF) DRIE recipe described in Table 4.4. A total of 80 cycles of passivation and etching, or 6.13 total minutes, is needed. Once the breakthrough is completed, etching will be stopped by the oxide layer at the device side of the wafer as demonstrated in Figure 4.3 d.

Table 4.3: Silicon oxide ICP RIE high etching rate recipe.

Parameters	**Settings**
Chamber Pressure	5mTorr
CHF_3 Gas Flow	40sccm
ICP Power	1500W
Generator Power	50W
Temperature	20˚C

Table 4.4: DRIE low frequency (LF) etching recipe.

Parameters	**Settings**
Chamber Pressure (Passivation/Etching)	24mTorr/30mTorr
SF_6 Gas Flow (Passivation/Etching)	0sccm/390sccm
C_4F_8 Gas Flow (Passivation/Etching)	250sccm/30sccm
O_2 Gas Flow (Passivation/Etching)	0sccm/39sccm
Passivation Duration per Cycle	2s
Etching Duration per Cycle	2.6s
Coil Power at 13.56MHz (Passivation/Etching)	2000W/2800W
Platen Power at 380KHz (Passivation/Etching)	0W/60W
Platen Power Modulation	80% Duty Cycle
Temperature	120˚C

As the SOI wafer is etched all the way through except for the thin oxide layer on the device side, the wafer must be attached to a carrier wafer using crystal bond to prevent leakage of gases through the wafer during etching steps.

The carrier wafer used must have a layer of silicon oxide on at least one surface. Crystal bonding is done by first depositing 0.5g of crystal bond material onto the non-oxide surface and degassing it in vacuum conditions at 70˚C. After degassing, place another carrier wafer, non-oxide side, on top of the carrier wafer with the crystal bond. Smear the two wafers so that crystal bond is evenly distributed across the surface. Reheat the wafer stack at 70˚C as needed if movement of the wafers becomes hindered. When the crystal bond is evenly coated, remove the two wafers

from each other thus creating two carrier wafers that are ready to be used in processing. Heat one of the wafers at 70˚C until the crystal bond is melted and place the substrate wafer on top of the crystal bond layer and move the two wafers around to spread the crystal bond across the substrate wafer. Put the stack into a vacuum at 70˚C and wait for at least 10 minutes. Remove the stack from the vacuum and use water and cleanroom wipes/polyester tips to clean away any excess crystal bond. It is imperative that crystal bond is completely wiped off the oxide surface of the carrier wafer.

The STS Pegasus ICP-DRIE, Figure 4.10, located in MNMS is used for all DRIE etching procedures. The tool is capable of etching silicon with a high etching rate of over 20μm/min. The tool uses C_4F_8 gas to deposit the passivation layer and SF_6 gas to etch the silicon. The tool is equipped with a 3000W coil power supply with RF frequencies of 13.56MHz and platen power supply at both 13.56MHz and 380KHz. The tool also uses oxygen gas which allows it to descum the sample by oxygen plasma etching right before DRIE etching.

The Oxford Instruments ICP RIE, Figure 4.11, located in the MNTL cleanroom is used for silicon oxide etching. This tool provides etching of oxide with high anisotropy.

Figure 4.10: The STS Pegasus ICP-DRIE in MNMS. The system on the right is the reaction chamber with a load chamber in the front. The computer program is used to set the etching recipe and perform operations. The left tower is the power regulator and supply for the system.

Figure 4.11: The Oxford Instruments ICP RIE in MNTL used to etch silicon oxide with high etching rate and selectivity.

4.2.5: Resulting Structure and Thin Film Membrane

At the end of the etching process, the plumbing structure will essentially be composed of two holes that are 400µm wide and 516µm deep with a thin oxide membrane of around 2.5µm thick on the device side. The membrane is very brittle due to the large 400µm wide area on which it is suspended and the thinness of the film itself, making it prone to breakage. Figure 4.12 shows optical images of intact and broken membrane.

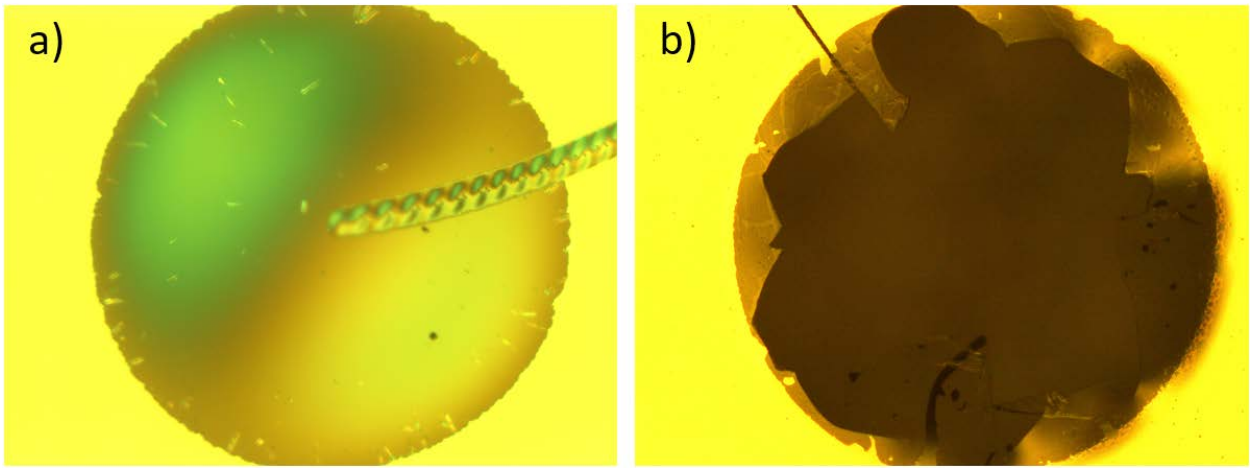

Figure 4.12: a) Intact oxide membrane as seen by the diffraction of the light due to the thin film oxide. b) Broken oxide membrane as seen by the cracking pattern and the lack of coloration.

To prevent breakage of the membrane in further processing, the substrate needs to remain bonded to the carrier wafer. As the membrane is on the device side, which is bonded to the carrier wafer, the carrier wafer provides a hard surface on which the membrane can lie, thus preventing breakage of the membrane in further processing.

4.3: Probe Fabrication

4.3.1: Process Overview

The probe shape itself needs to be patterned and etched after the plumbing holes are fabricated. The general process is shown in Figure 4.13. The trenches that define the outline of the probe are 20µm wide on the device side and 35µm wide on the handle side to allow for an alignment tolerance of 15µm. After undergoing the processing step, the release probes will remain attached to the wafer through four 100µm wide device-side silicon, 15µm thick, bridges. This allows for transfer of the probes as a wafer until needed.

4.3.2: Plumbing Hole Protection

As seen in the fabrication flow in Figure 4.13, the SOI wafer is required to undergo another round of etching on the handle side thus requiring protection for the thin oxide membrane formed on top of the plumbing holes.

The protection is accomplished by plugging the plumbing holes with KMPR photoresist as shown in Figure 4.13 a. As the holes are relatively deep, spin coating the KMPR is not possible and the resist will not flow down into the holes. Spreading KMPR physically will allow the KMPR to flow into the holes thus plugging the plumbing holes. To accomplish this, first deposit in bulk KMPR photoresist onto the handle side of the SOI wafer. Evenly spread the resist with a brush made with PDMS or any rubbery material with a flat edge. Let the resist sit for 5 minutes on the wafer and then use the flat edge of the brush to brush off any excess KMPR resist leaving only a thin flat layer. Soft bake the substrate with resist for 5 minutes at 110˚C with a cover.

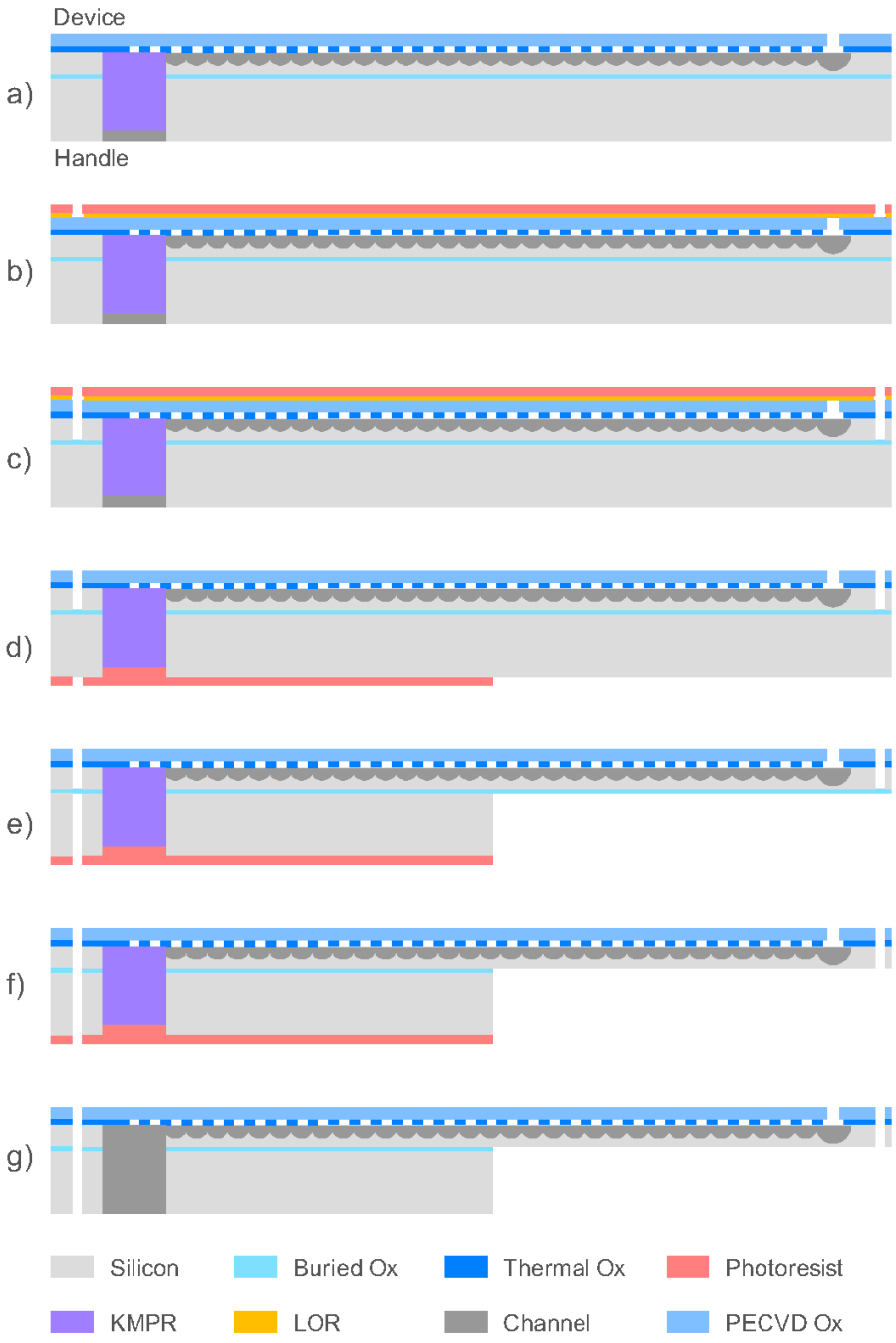

Figure 4.13: Cross-section schematic of probe fabrication. a) KMPR photoresist is coated and exposed to create plugs for the plumbing holes to protect the oxide membrane on the device side from further etching and breakage in remaining processing steps. b) Lift-off resist and photoresist are spin coated and patterned with the probe outline on the device side of the SOI wafer. c) The outline of the probe on the device side is etched through the deposited oxide from channel fabrication and the device-side silicon to the BOx. d) The device-side photoresist stack is stripped off and a layer of photoresist is spin coated onto the handle side and patterned with the outline of the probe. The KMPR plug will also help with planarization of the resist on this side of the substrate. e) The handle-side silicon patterned with the probe outline is etched with DRIE to the BOx layer. f) The BOx located at the probe outline is etched away with ICP RIE thus releasing the neuroprobe from the SOI wafer. g) The photoresist and KMPR plugs are stripped away finishing the processing step.

The resist is then exposed with the EV620 aligner described in Section 4.2.3 using the same mask that contains the plumbing hole features. Top-side contact lithography in hard contact mode is used and the power setting is 300mJ/cm^2. Post exposure bake is for 2 minutes at 110˚C. Develop the resist for 2 minutes with SU8 developer and rinse with IPA after development. As KMPR is a negative photoresist, the re-exposure of the plumbing hole features will result in the resist within the plumbing holes to cross-link to form plugs. KMPR on the surface of the wafer that is not exposed is washed away by the developer creating a smooth surface for subsequent photoresist coating. Figure 4.14 shows the cross-section image of the plumbing holes with the KMPR plug. Heat up the substrate stack and slide the SOI wafer off the carrier wafer and submerge it in DI water at 80˚C for 10 minutes or until all crystal bond is dissolved away. The membrane will now have the KMPR plug as support to prevent breakage of the oxide membrane.

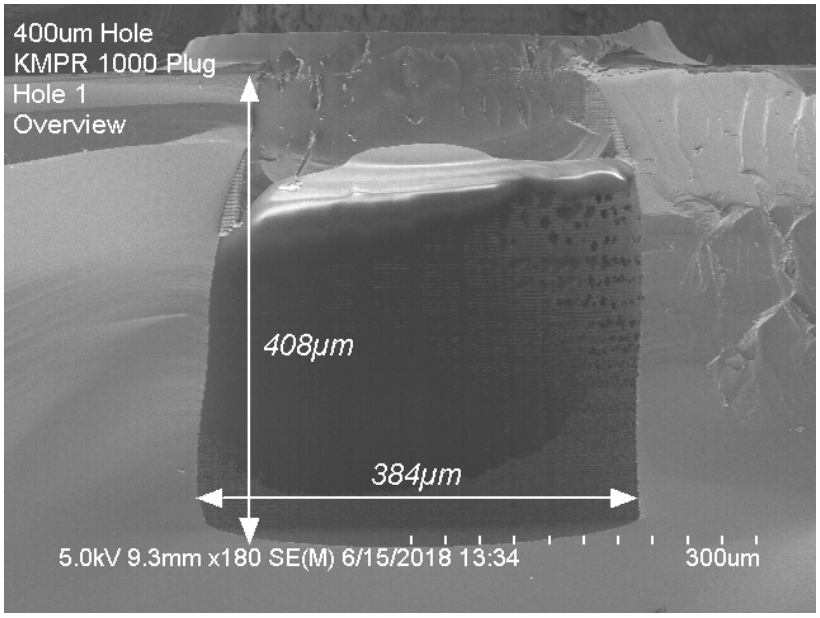

Figure 4.14: Plumbing hole with KMPR plug. The plug fills the holes at the bottom thus protecting to the material at the bottom from further etching.

4.3.3: Device-Side Probe Etch

The device side of the wafer needs to be patterned with the outline of the probe as shown by the mask pattern in Figure 4.15. Twenty-micron-wide lines outline the shape of the 2cm by 2cm square base and the needle with width of 55µm at the tip and 75µm at the base. The outline at the base is cut off at four points to create the 100µm bridges used to connect the probe to the wafer at the end of processing.

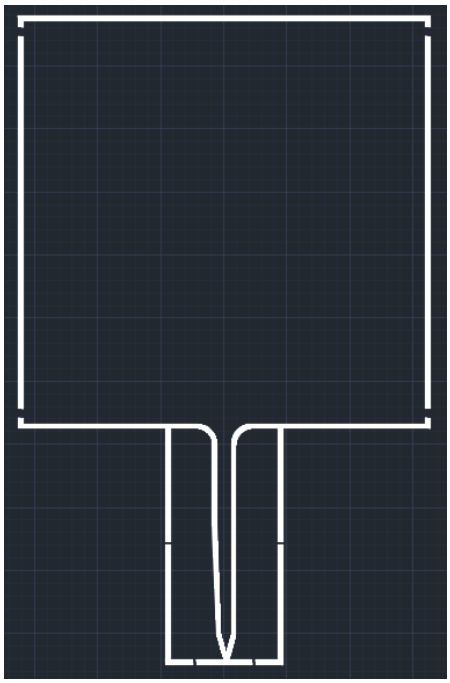

Figure 4.15: Probe outline features on device side. The four breakages in the outline of the base create thin silicon bridges between the neuroprobe base and the wafer allowing it to remain attached to the wafer until needed.

Bond the SOI wafer to a carrier wafer using crystal bond on the handle side of the wafer. This is done to ensure no gas leakage occurs during etching from any cracks in the oxide membrane at the plumbing holes. LOR-10A is then first spin coated onto the device side of the SOI wafer. Cover the whole wafer surface with the lift-off resist to reduce the comet pattern caused by the plumbing holes. The spin coat recipe is done in two steps as shown in Table 4.2. SPR220 is then spin coated onto the device side of the SOI wafer using the recipe as shown in Table 4.1. As was done with the lift-off resist, cover the whole wafer with the resist to reduce the comet pattern. Soft bake is at 60˚C for 2 minutes followed by another minute of baking at 110˚C. The resist is exposed with contact exposure on the EV620 aligner using hard contact mode. Top-side alignment is performed to align the channel to the structures of the probe. The exposure energy used is 200mJ/cm^2, and exposure is followed by a 25 seconds development in the AZ 917 MIF developer. Only agitate the wafer for 5 seconds before taking it out of the developer. The lithography results are shown in Figure 4.13 b.

After photolithography, the 2.5µm thick oxide on the device layer is etched off with the Oxford ICP RIE recipe described in Table 4.3 for 25 minutes. After the oxide is removed, the LF DRIE etching process described in Table 4.4 is performed to etch away the device silicon to the

BOx layer to achieve the structure shown in Figure 4.12 f. A total of 66 cycles of passivation and etching, or 5.06 total minutes, are needed to complete the etching process and produce the structure shown in Figure 4.13 c.

Remove the substrate from the carrier wafer and clean the wafer of crystal bond. Use Microposit Remover 1165 photoresist stripper to strip away the photoresist from the lithography step using the process described in Section 4.2.4.

4.3.4: Handle Side Probe Etch

The last step of the process etches the probe shape onto the handle side of the wafer. Figure 4.16 shows the mask pattern used in the lithography in this process step. The features consist of the shape of the 2cm by 2cm square base with the trench being 35µm wide. At the probe area, a large rectangle with dimensions of 1.2mm by 0.6mm is patterned and etched. This large area allows the needle to be released without the need of side etching the BOx to remove the handle-side silicon and allows for more mis-alignment tolerance.

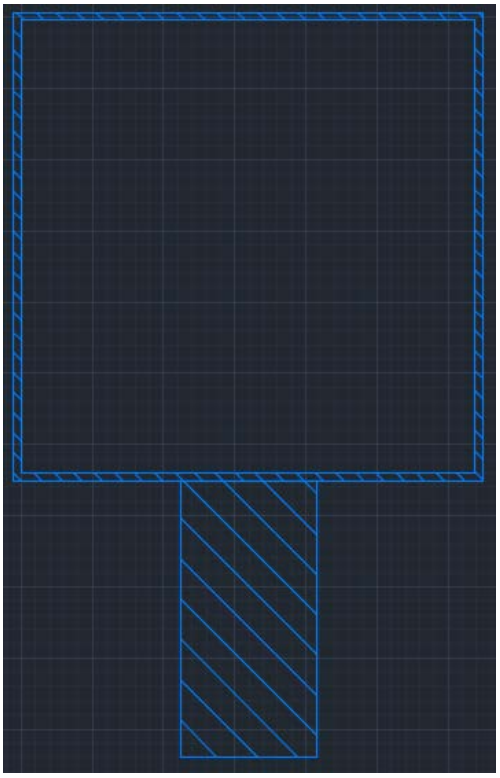

Figure 4.16: Probe outline features on handle side. The outline goes around the base thus ensuring only device-side silicon will be used as the bridge. The large rectangle feature allows the needle to be released without need of chemical side etching of the BOx and reduces the chance of breakage of the needle by the weight of the handle-side silicon.

Spin coat SPR220 photoresist with the recipe in Table 4.1. Like the previous spin coating step, cover the whole wafer with the resist to prevent the comet pattern. Soft bake the resist at 110˚C for 1 minute. Perform bottom-side alignment to align the mask probe features to those on the front. Use the EV620 contact aligner as described in Section 4.2.3 for bottom-side alignment with an exposure energy of 200mJ/cm^2. Develop the resist for 1 minute using AZ 917 MIF developer and quench in DI water for 1 minute. The resulting pattern should look like that in Figure 4.13 d.

Bond the substrate on the device side to a carrier wafer with crystal bond. Perform DRIE etching with the STS Pegasus using the high-frequency recipe shown in Table 4.2. A total of 222 cycles of passivation and etching, or 35.7 total minutes, is needed for the etch process. This procedure will etch the exposed silicon all the way to the buried oxide level leaving the structure shown in Figure 4.13 e. As the plumbing holes are plugged up with KMPR resist, this etching step will protect the thin oxide membrane from being etched and damaged. After processing, the probe is now attached to the wafer through the BOx layer in the probe outline and the silicon bridges.

4.3.5: Probe Release

Use Oxford Freon ICP RIE to etch away the exposed BOx in the probe outline trenches from the handle side. The standard MNTL high-etch-rate recipe is used and is etched for 7.5 minutes. After this etch, the probe will be completely released from the substrate, Figure 4.13 f, except for the thin silicon bridges.

Remove the substrate carefully from the carrier wafer and submerge it in DI water at 80˚C until crystal bond is dissolved. After removing the crystal bond, strip the photoresist with Microposit Remover 1165 photoresist stripper in two baths at 80˚C for at least 10 minutes to completely remove both the KMPR plugs and the resist to finish the fabrication process as shown in Figure 4.13 g. Figure 4.17 shows the results of complete removal of the plugs where no additional silicon is etched from the DRIE process in Section 4.3.4.

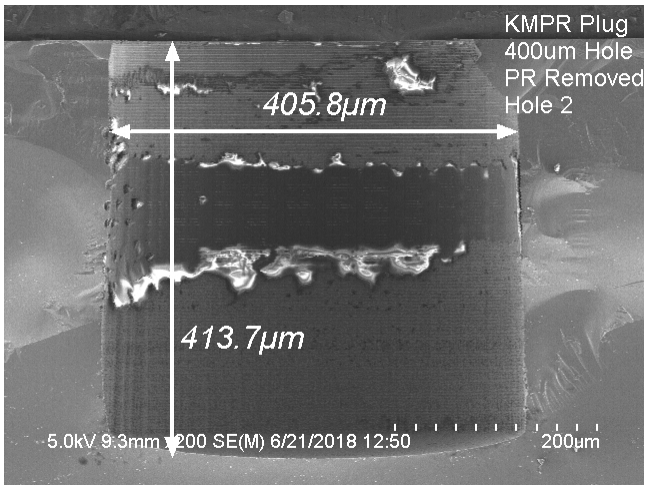

Figure 4.17: Plumbing hole after DRIE and ICP RIE processing and with the KMPR plug stripped away. The overall depth of the hole is of the same order as that in Figure 4.14 thus demonstrating the KMPR plug's ability to protect the thin film oxide on top of the plumbing hole.

Figure 4.18 shows the general floorplan of the probes on the die. To release a single probe from the substrate, the left-side silicon is first snapped off along the tapper to expose the probe base edge. To remove a single probe, use a tweezer and hold the exposed base edge and snap up the probe to break the silicon bridge on the right to fully release the probe and needle from the wafer.

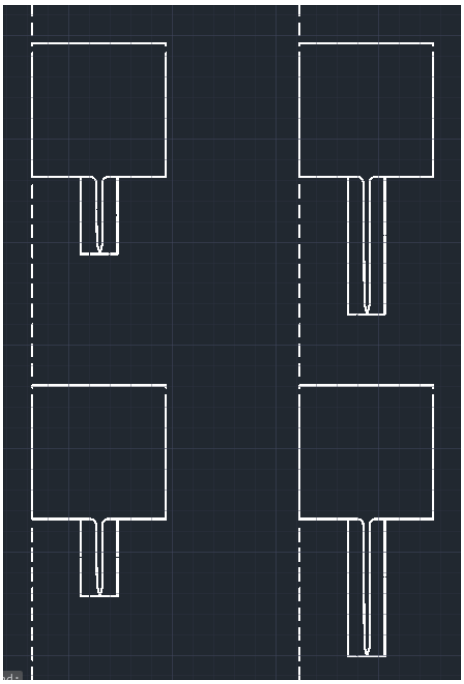

Figure 4.18: The floorplan of multiple probes on the mask die. The tapered line along the left side of the probe allows for easy snap-off of a column of probe. Once a column is free from the substrate, the base of the individual probe can be accessed and released with a simple snap of the probe upward.

4.3.6: Released Probe Results

Figure 4.19 shows SEM images of the released probes. As seen, the needle and tip are clearly etched into the silicon. As can be seen in the images, the needle experiences downward bending due to the high tensile stress from the deposited oxide from the channel fabrication process. The bending can be reduced by adding a compressively stressed film such as silicon nitride to compensate for the downward stress experienced by the needle. Figure 4.20 shows needles fabricated with the oxide and nitride stack with the oxide being 2.5µm and nitride being 200nm thick. The needle with the stack films is seen to have barely any bending. Figure 4.21 shows the intrinsic stress of various oxide and nitride films that are measured as part of the stress engineering process to achieve a straight needle.

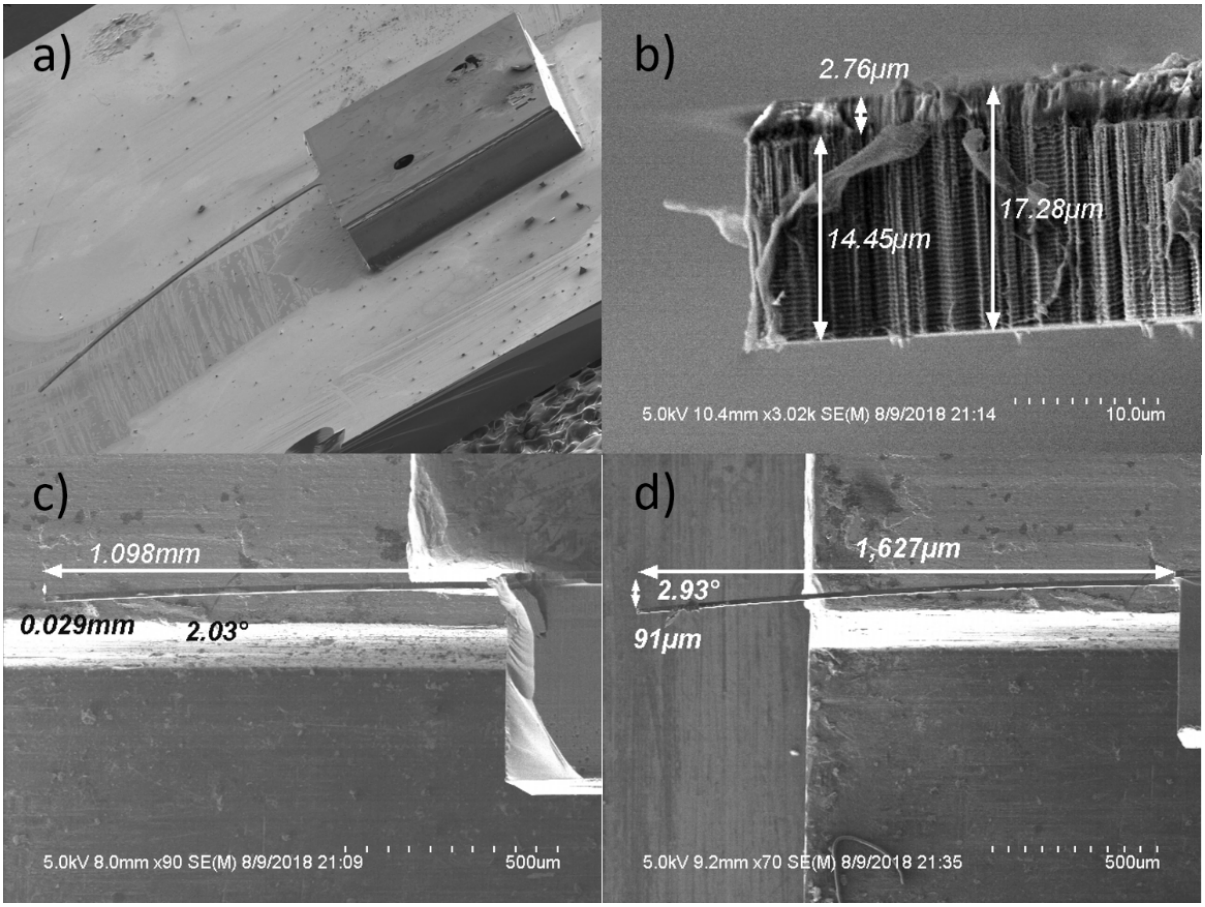

Figure 4.19: SEM pictures of released neuroprobe. a) Released probe showing the base and the needle. The needle can be seen to be bending due to the tensile stress from the deposited oxide layer. b) Thickness of needle at the tip. The resulting thickness is as expected. c) Side view of 1mm needle showing appreciable bending due to the deposited oxide stress. d) Side view of 1.5mm needle showing greater bending than that of 1mm needle. As the length of the needle increases, more bending is observed thus potentially limiting the length of needle that can be safely fabricated.

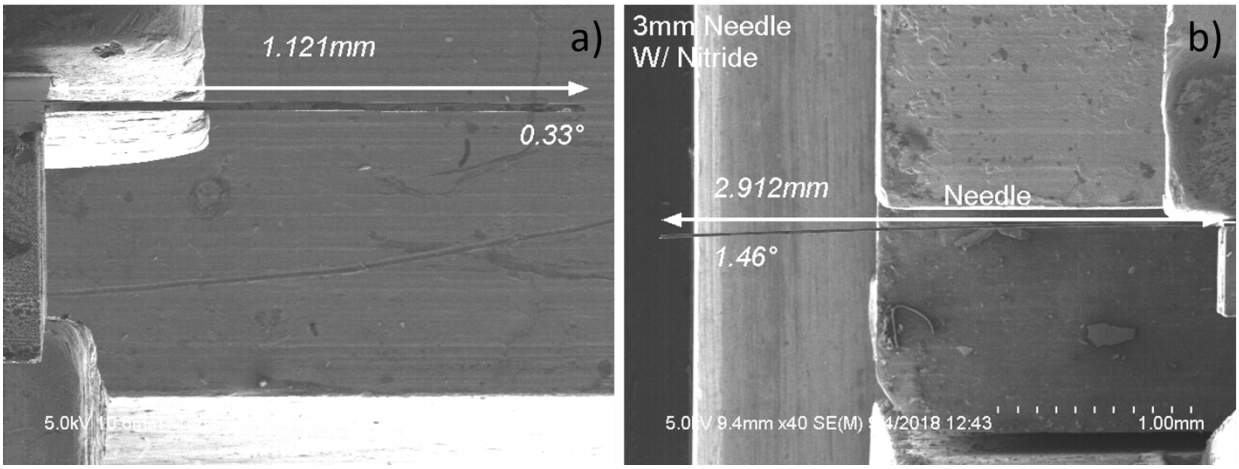

Figure 4.20: Side view of needles with a 2.5µm oxide and 200nm nitride thin film stack. a) 1mm long needle shows significantly less bending compared to the needle with only the oxide film. The needle is essentially straight. b) 3mm needle exhibiting some bending. The bending from this long needle is smaller than that of the 1mm needle with only the oxide, thus showing that an oxide – nitride thin film stack is capable to be stress engineered to compensate for the intrinsic stress of the materials.

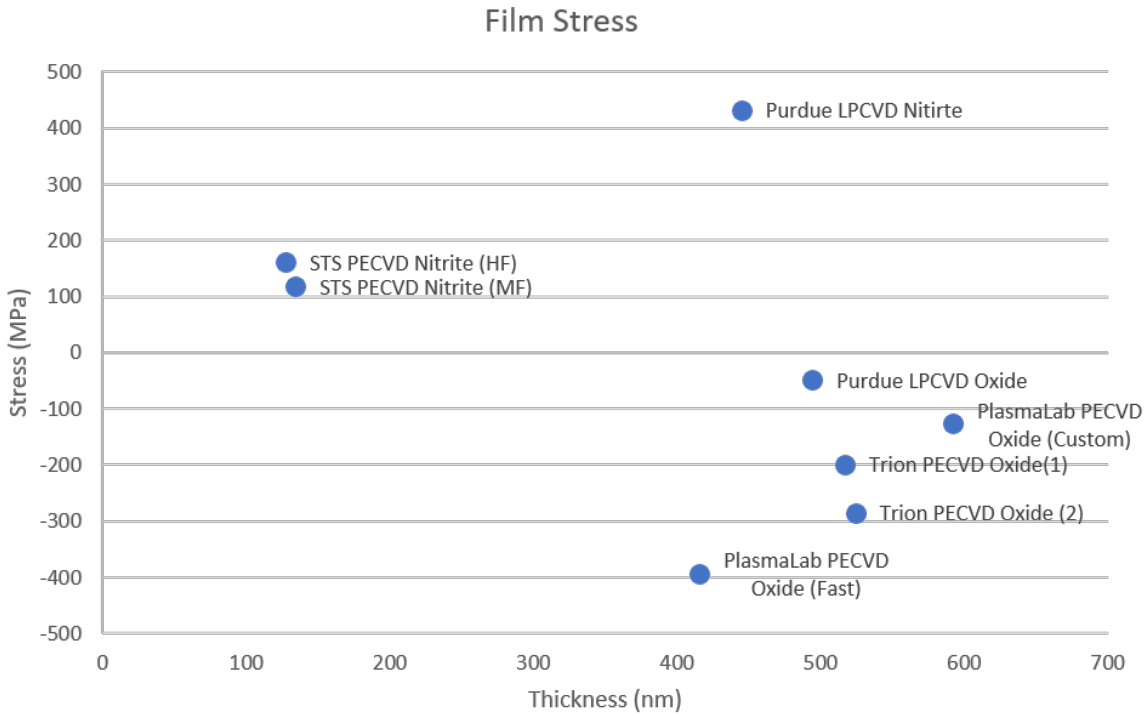

Figure 4.21: Graph showing the thickness and stress of multiple thin oxide and nitride films tested for stress engineering. PECVD films are deposited in MNTL while LPCVD films are deposited at Purdue University.

Chapter 5: Probe Packaging

5.1: Packaging Overview

The probes are packaged by inserting glass capillaries into plumbing structures etched into the base of the probe. The capillaries purchased from Molex have an outer diameter of 360µm and an inner diameter of 250µm. After insertion, the capillaries are sealed with epoxy. As the capillaries are placed very close to each other, both capillaries must be inserted together simultaneously. To accomplish this, a setup with micromanipulators is made to provide fine alignment of the capillaries to the plumbing structures. The two capillaries are inserted simultaneously with the aid of a 3D printed holder that also acts as a handle for the neuroprobe.

5.2: 3D Printed Holder

A holder design is shown in Figure 5.1. The holder is designed using Autodesk Inventor 3D CAD program and has dimensions of 8.5mm by 2mm by 15mm in width, height, and length respectively. The holder contains two screw holes with diameters of 2mm that are placed in series with 5mm separation. These two holes allow for the holder to be screwed at a straight angle onto the manipulator setup.

The holder contains two parallel rectangular grooves with width of 0.4mm and height of 0.6mm. The grooves run through the whole length of the holder and are open at both ends. The grooves are separated by 1.042mm matching the separation of the plumbing structure on the neuroprobe.

The holder is 3D printed with clear resin using stereolithography (SLA) 3D printing technology. SLA uses a finely focused laser to perform controlled photopolymerization of resin in a layer-by-layer fashion to create finely detailed features such as those needed by the grooves. The holders are printed by the Rapid Prototyping Lab located in the Mechanical Engineering Lab at the University of Illinois at Urbana-Champaign using the Viper SI SLA 3D printer.

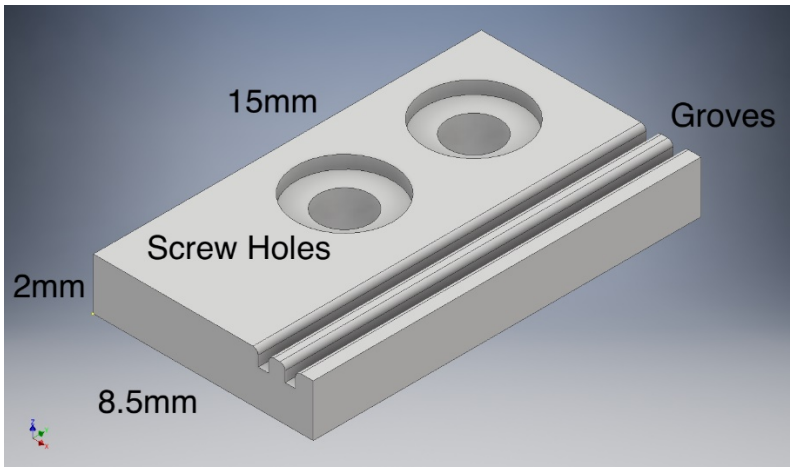

Figure 5.1: 3D printed holder with grooves for capillary separation. The holder allows for simultaneous insertion of both capillaries into the probe. The holder also acts as the handle for the probe.

5.3: Capillary Insertion Setup

The capillaries are precisely aligned and inserted into the plumbing holes of the neuroprobes with a three-axis micromanipulator and a rotational stage. The setup is shown in Figure 5.2. The micromanipulators are purchased from Thorlabs and consist of three 25mm travel stages set up to move in the x, y, and z direction. A long rod is attached to the three-axis micromanipulator parallel to the ground. The extruded end of this rod is where the 3D printed holder will be attached to with two screws to ensure that the capillaries are parallel to the ground.

The probe sits on a rotation stage and is parallel to the ground. This setup thus ensures that the capillaries will always be inserted into the plumbing holes on the probe at a right angle. The rotational stage is used to align the holes with the capillaries along the x-axis.

A handheld microscope is used to magnify the area around the plumbing structures on the probe to allow for the precise alignment of the capillaries to the holes. The Supereyes B011 is used in this setup. The microscope has a 5MP camera and with the L100 lens, has a magnification factor of 30x to 300x and working distance of 30-200mm that allows the microscope to be placed farther away from the congested area around the neuroprobe in the setup.

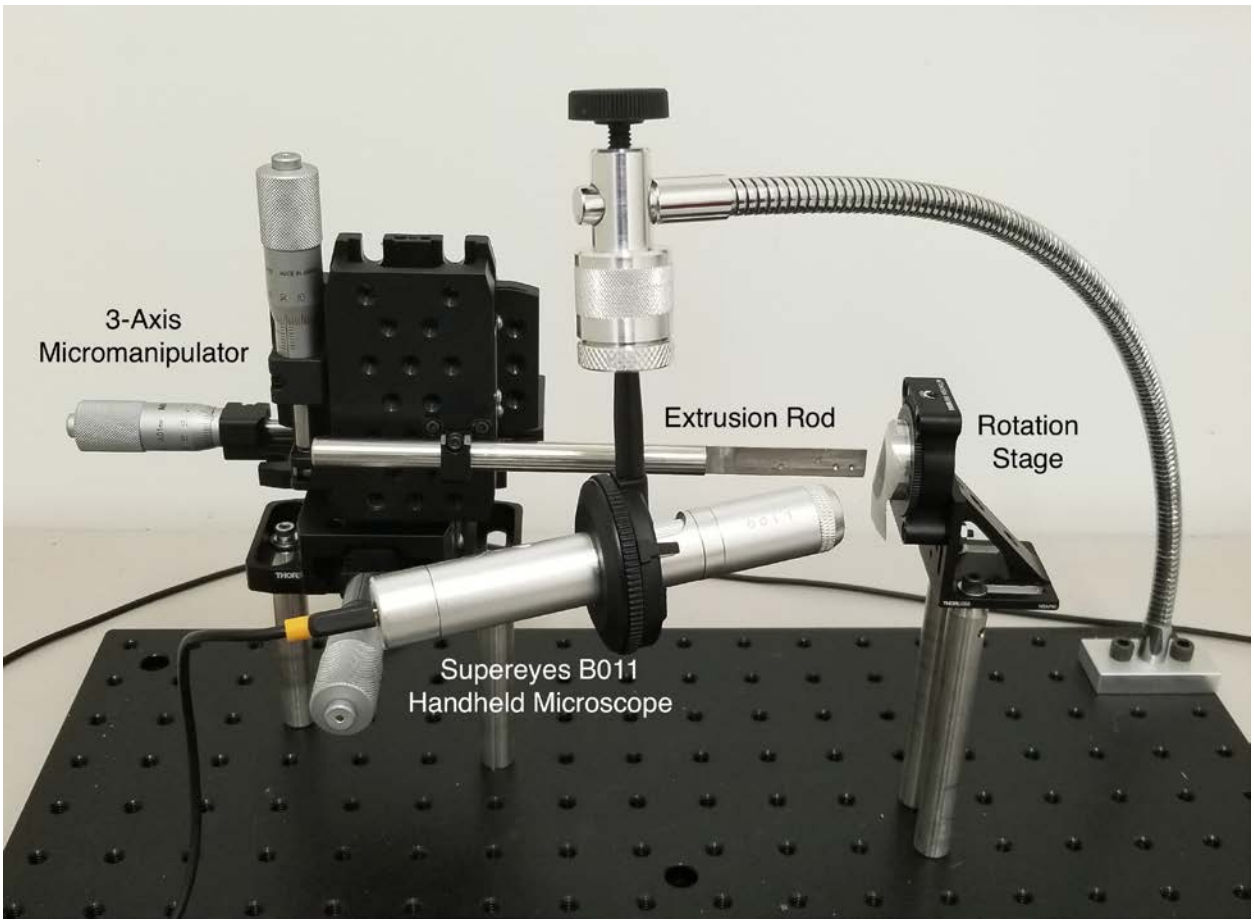

Figure 5.2: The setup used to package the neuroprobe with plumbing. The setup gives four degrees of freedom to align the capillaries with the plumbing holes. The handheld microscope is used to give more viewing angle and easier access to the stage compared to traditional microscopes. The rotation stage contains a step that allows the needle of the probe to hang in the air to prevent breakage of the needle.

5.4: Package Procedure

Start the packaging process by cutting two pieces of the glass capillaries. Place the two capillaries into the two grooves. Let the capillaries extrude out from one end of the holder by about 1mm while making sure the two ends are flush with each other. Apply epoxy to the surface of the holder to glue the capillaries onto the 3D printed holder. When the epoxy is dry, insert the other end of the capillaries into plastic tubing with inner diameter of 0.4mm. and apply epoxy to seal the plastic tubing and capillary joint. The resulting structure should look like that shown in Figure 5.3.

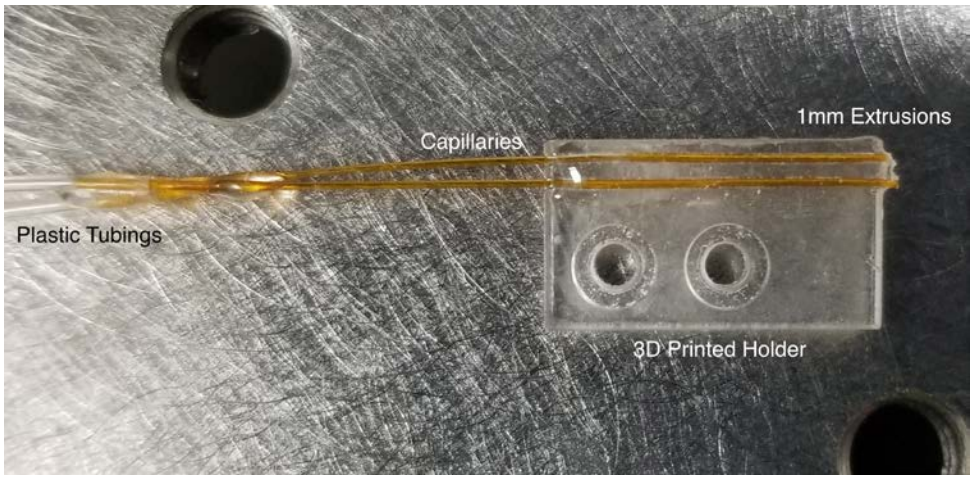

Figure 5.3: Assembled 3D printed holder with capillaries and plastic tubing held together with epoxy.

Attach the holder onto the rod extruded from the manipulator with two screws and the 1mm capillary extrusions from the holder facing toward the sample stage. Use double-sided tape and attach the device side of the probe base to the stage. The stage has a step to allow the needle to hang in air. It is imperative that only the base is attached to the stage as the needle will break when removing the probe from the adhesive.

Use the 3-axis manipulator and the rotational stage to align the capillaries to the plumbing holes as shown in Figure 5.4. Once the capillaries are inserted into the plumbing holes on the probe, use epoxy to seal capillaries and the plumbing holes on the probe. Once the epoxy is dry, carefully unscrew the holder from the rod and remove the probe from the state to obtain the final package neuroprobe shown in Figure 5.5.

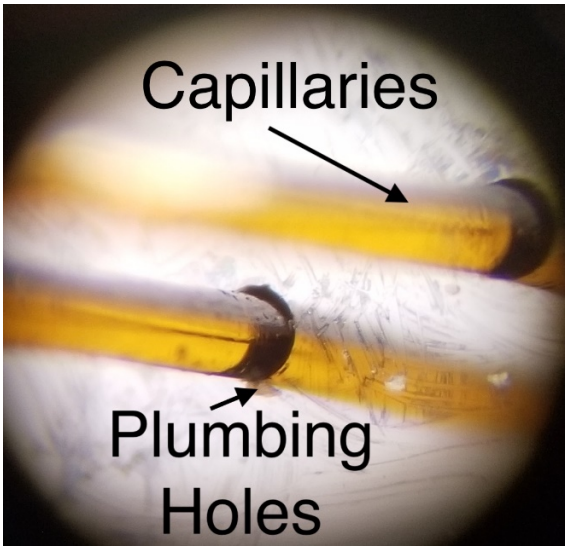

Figure 5.4: Capillaries inserted into plumbing holes using the setup shown in Figure 5.2.

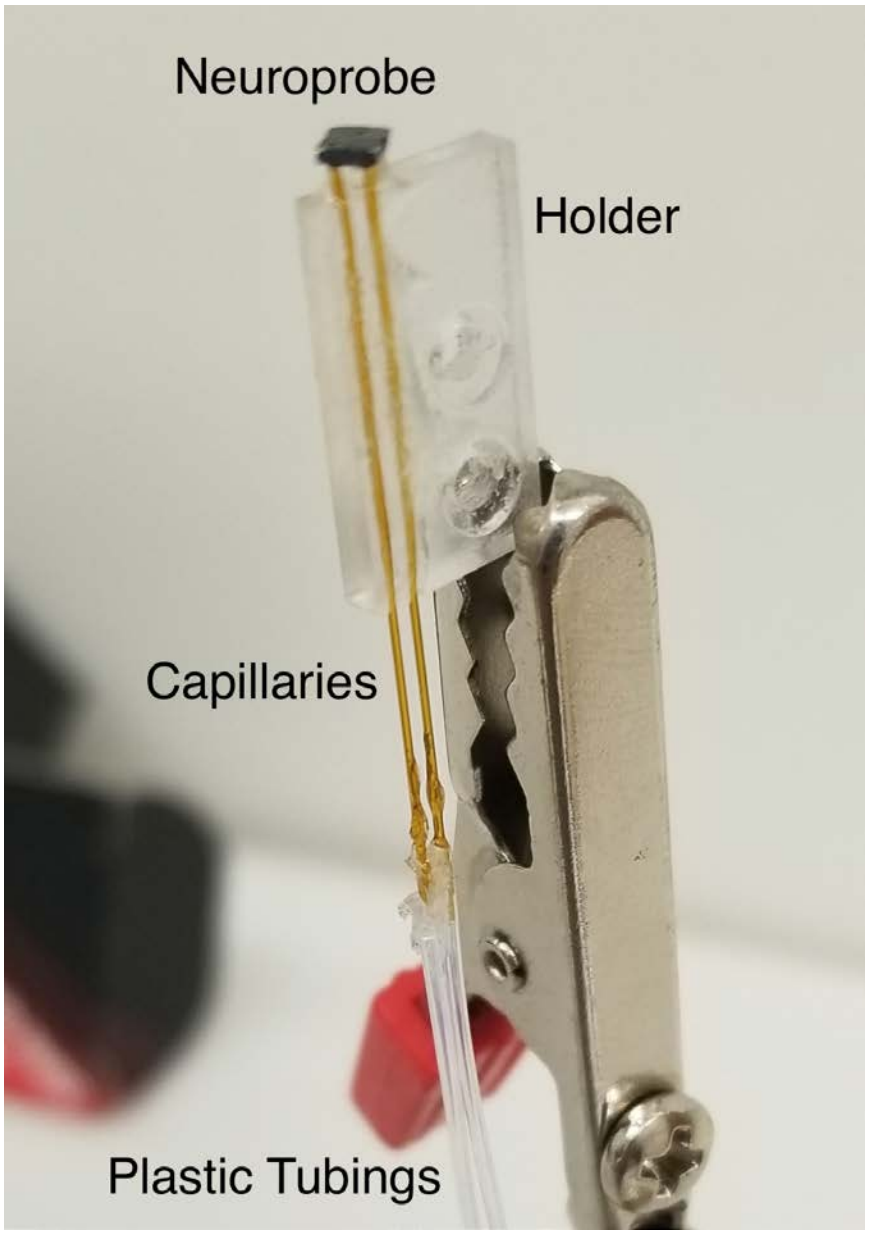

Figure 5.5: Packaged neuroprobe with inserted capillaries and tubing for plumbing and holder as the handle.

Chapter 6: Future Developments

The fabrication and packaging process described in Chapter 4 and Chapter 5 results in silicon microfluidic neuroprobes that are packaged and ready to be tested in simulated environments. The process, however, does have two major drawbacks that limit the yield rate of the fully functional neuroprobe. The first is the breakage of oxide thin film on top of the plumbing holes and the second is the imprecision of the packaging method. These two issues need to be addressed in future developments and will be discussed briefly in this chapter.

Thin oxide film breakage is responsible for a majority of the defects found in processed probes. The yield rate with both membranes remaining intact is found to be only 20%. It is understandable that the membrane is very brittle due to the large area covered and the thinness of the film. To improve the yield of the probe, a process needs to be developed to reduce the area of the thin film membrane. One way to reduce the area is to etch through the silicon between the channel and the BOx from the device side of the SOI wafer instead of from the handle side. Doing this restricts the large hole area, 400μm in diameter, to only the handle side of the substrate while the thin membrane will only be suspended over an opening on the order of tens of microns due to isotropic etching of XeF_2 used to etch device-side silicon. Figure 6.1 shows the schematics for the proposed process.

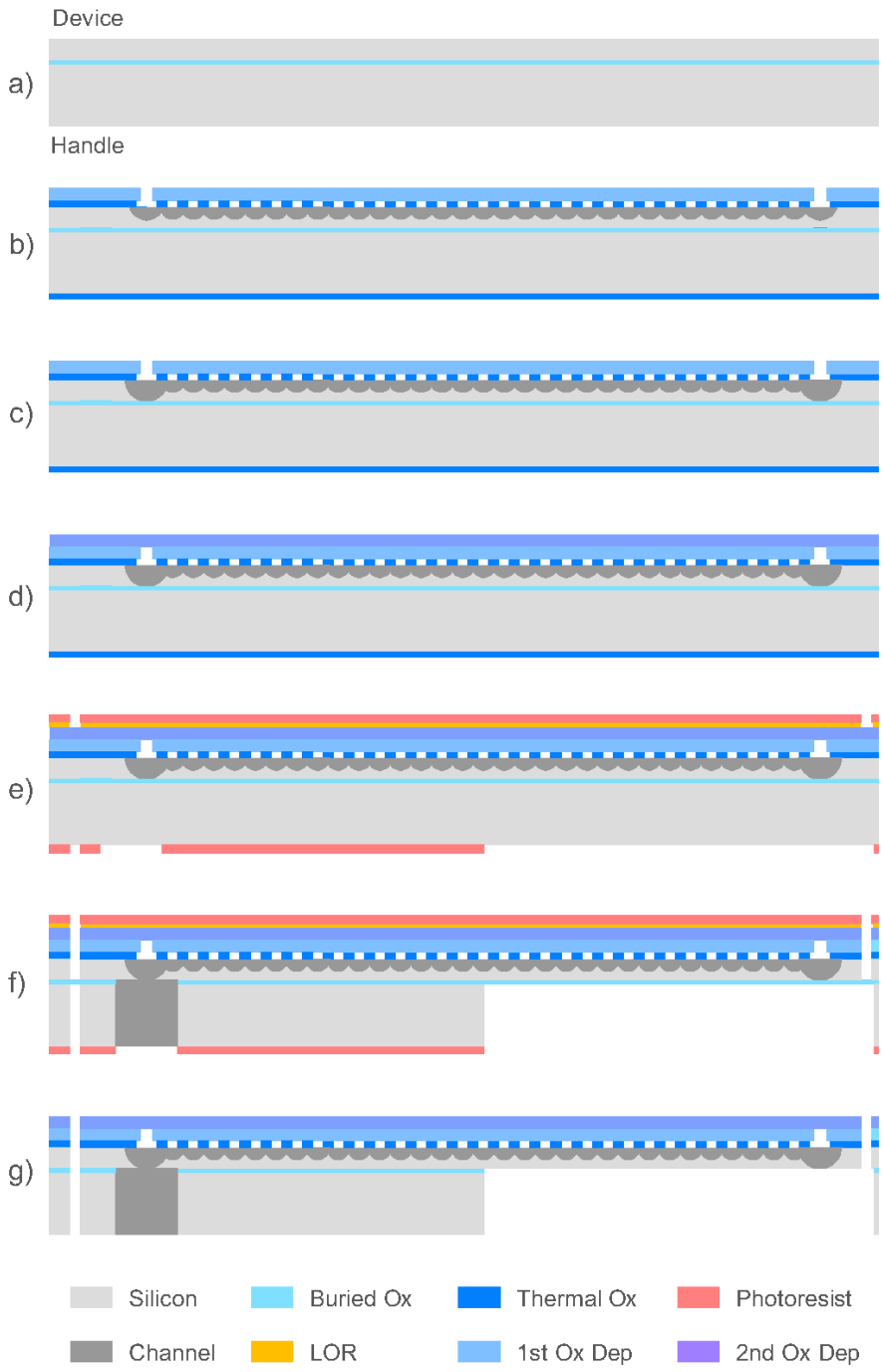

Figure 6.1: Cross-section schematic view of proposed fabrication process. This process results in the opening at the end of the needle being placed on the bottom instead of the top and also limits the size of the oxide membrane to prevent breakage during processing. a) SOI wafer is used as the substrate. b) Bulk silicon channel fabricated using the steps described in Figure 4.2. The features at the two ends of the channel are designed to be larger than that along the channel to ensure that it does not seal during the first oxide deposition. c) As the ends of the channels are not sealed off, the silicon at the ends can be further etched with XeF_2 until the BOx layer. d) A second oxide layer is deposited on the device side to seal off the openings at the ends of the channel. e) Photoresist is patterned to have the probe outline on the device side and the probe outline and plumbing structure on the handle side in one mask layer. f) ICP RIE and DRIE are performed to etch the resist pattern into the SOI substrate. g) The exposed BOx layer is etched away using ICP RIE and the resists are stripped to produce the neuroprobe.

To address the second issue, a new method is being developed to attach capillaries to the 3D printed holder. Figure 6.2 shows the process to create the holder setup. This holder spaces out capillaries with other capillaries in between. The spacing capillary is also moved back from the end of the protruding capillaries by 360µm allowing them to become natural stops in the insertion process thus preventing capillaries from going through the wafer and damaging device-side channels. The process described in Figure 6.1 also has a natural stop built into the wafer itself by the mismatch of dimensions between the plumbing holes on the handle-side and device-side silicon. These two improvements to the packaging system should prevent capillaries from damaging the neuroprobes as well as reduce chances of debris and epoxy blocking off fluid flow between the capillaries and the channels.

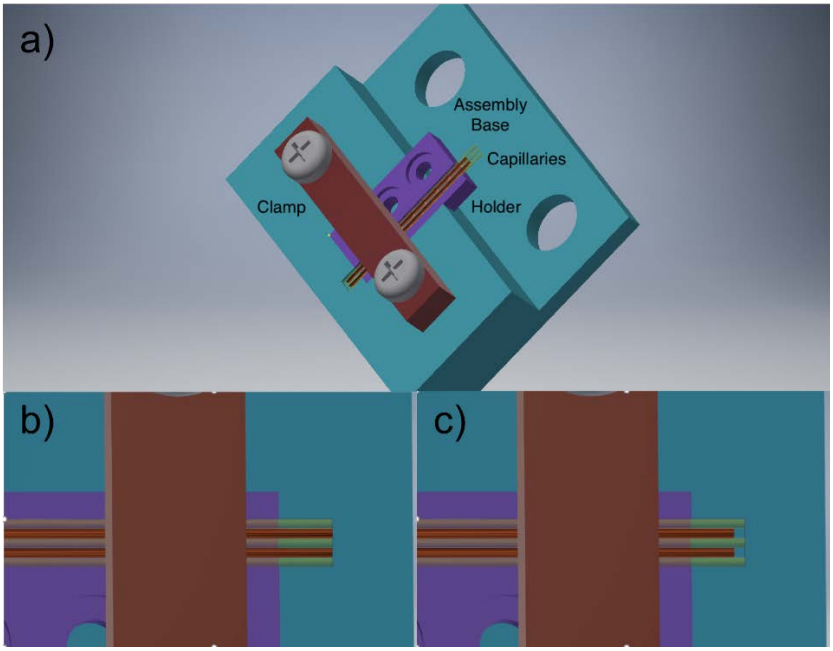

Figure 6.2: Assembly to make proposed holder with capillaries (yellow) separated out using spacer capillaries (orange). a) Assembly when everything has been put together. Start the assembly by first placing the 3D printed holder onto the assembly base as shown. The holder now has one large rectangular area to accommodate both the capillaries and the spacers. Put both the insertion and spacer capillaries onto the holder and screw on the clamp. Push all the capillaries into the groove on the assembly base making the ends flash against the wall as shown in b). Use a needle with diameter of 0.36mm and push the spacer capillaries back as shown in c). Apply epoxy to the holder and the capillaries to hold them together. Remove the clamp and the holder when the epoxy has dried. The spacer capillaries now act as natural stops when inserted into the neuroprobes thus allowing the capillaries to only go down by 0.36mm.

The two described improvements to the fabrication and packaging process should increase overall yield and functionality of the microfluidic neuroprobes that will ultimately be used as an essential tool in large research projects into the cognitive processing of the brain.

References

[1] L. F. Agnati, G. Leo, A. Zanardi, S. Genedani, A. Rivera, K. Fuxe, and D. Guidolin, "Volume transmission and wiring transmission from cellular to molecular networks: history and perspectives," *Acta Physiologica*, vol. 187, no. 1-2, pp. 329–344, 2006.

[2] E. Syková and C. Nicholson, "Diffusion in Brain Extracellular Space," *Physiological Reviews*, vol. 88, no. 4, pp. 1277–1340, 2008.

[3] L. Xie, H. Kang, Q. Xu, M. J. Chen, Y. Liao, M. Thiyagarajan, J. Odonnell, D. J. Christensen, C. Nicholson, J. J. Iliff, T. Takano, R. Deane, and M. Nedergaard, "Sleep drives metabolite clearance from the adult brain," *Science*, vol. 342, no. 6156, pp. 373–377, 2013.

[4] B.-J. Jin, A. J. Smith, and A. S. Verkman, "Spatial model of convective solute transport in brain extracellular space does not support a 'glymphatic' mechanism," *The Journal of General Physiology*, vol. 148, no. 6, pp. 489–501, Nov. 2016.

[5] Q.-T. Nguyen, L. F. Schroeder, M. Mank, A. Muller, P. Taylor, O. Griesbeck, and D. Kleinfeld, "An in vivo biosensor for neurotransmitter release and in situ receptor activity," *Nature Neuroscience*, vol. 13, no. 1, pp. 127–132, 2009.

[6] S. A. Hires, Y. Zhu, and R. Y. Tsien, "Optical measurement of synaptic glutamate spillover and reuptake by linker optimized glutamate-sensitive fluorescent reporters," *Proceedings of the National Academy of Sciences*, vol. 105, no. 11, pp. 4411–4416, Oct. 2008.

[7] J. S. Marvin, B. G. Borghuis, L. Tian, J. Cichon, M. T. Harnett, J. Akerboom, A. Gordus, S. L. Renninger, T.-W. Chen, C. I. Bargmann, M. B. Orger, E. R. Schreiter, J. B. Demb, W.-B. Gan, S. A. Hires, and L. L. Looger, "An optimized fluorescent probe for visualizing glutamate neurotransmission," *Nature Methods*, vol. 10, no. 2, pp. 162–170, 2013.

[8] J. Duarte-Neves, L. P. D. Almeida, and C. Cavadas, "Neuropeptide Y (NPY) as a therapeutic target for neurodegenerative diseases," *Neurobiology of Disease*, vol. 95, pp. 210–224, 2016.

[9] E. S. Bucher and R. M. Wightman, "Electrochemical analysis of neurotransmitters," *Annual Review of Analytical Chemistry*, vol. 8, no. 1, pp. 239–261, 2015.

[10] R. M. Wightman, "Probing cellular chemistry in biological systems with microelectrodes," *Science*, vol. 311, no. 5767, pp. 1570–1574, 2006.

[11] M. Ganesana, S. T. Lee, Y. Wang, and B. J. Venton, "Analytical techniques in neuroscience: recent advances in imaging, separation, and electrochemical methods," *Analytical Chemistry*, vol. 89, no. 1, pp. 314–341, 2016.

[12] V. Castro, C. Valenzuela, J. Sanchez, K. Pena, S. Perez, J. Ibarra, and A. Villagran, “An update of the classical and novel methods used for measuring fast neurotransmitters during normal and brain altered function,” *Current Neuropharmacology*, vol. 12, no. 6, pp. 490–508, 2015.

[13] W. H. Lee, T. R. Slaney, R. W. Hower, and R. T. Kennedy, “Microfabricated sampling probes for in vivo monitoring of neurotransmitters,” *Analytical Chemistry*, vol. 85, no. 8, pp. 3828–3831, Mar. 2013.

[14] B. Spengler, “Mass spectrometry imaging of biomolecular information,” *Analytical Chemistry*, vol. 87, no. 1, pp. 64–82, 2014.

[15] E. V. Romanova, J. T. Aerts, C. A. Croushore, and J. V. Sweedler, “Small-volume analysis of cell–cell signaling molecules in the brain,” *Neuropsychopharmacology*, vol. 39, no. 1, pp. 50–64, Oct. 2013.

[16] P. Nemes, S. S. Rubakhin, J. T. Aerts, and J. V. Sweedler, “Qualitative and quantitative metabolomic investigation of single neurons by capillary electrophoresis electrospray ionization mass spectrometry,” *Nature Protocols*, vol. 8, no. 4, pp. 783–799, 2013.

[17] J. T. Aerts, K. R. Louis, S. R. Crandall, G. Govindaiah, C. L. Cox, and J. V. Sweedler, “Patch clamp electrophysiology and capillary electrophoresis–mass spectrometry metabolomics for single cell characterization,” *Analytical Chemistry*, vol. 86, no. 6, pp. 3203–3208, Jun. 2014.

[18] B. H. C. Westerink and T. I. F. H. Cremers, *Handbook of Microdialysis: Methods, Applications and Perspectives*, 1st ed. Amsterdam; Boston: Elsevier Academic Press, 2007, pp. 697.

[19] H. Gu, E. L. Varner, S. R. Groskreutz, A. C. Michael, and S. G. Weber, “In vivo monitoring of dopamine by microdialysis with 1 min temporal resolution using online capillary liquid chromatography with electrochemical detection,” *Analytical Chemistry*, vol. 87, no. 12, pp. 6088–6094, 2015.

[20] T. Ngernsutivorakul, D. J. Steyer, A. C. Valenta, and R. T. Kennedy, “In vivo chemical monitoring at high spatiotemporal resolution using microfabricated sampling probes and droplet-based microfluidics coupled to mass spectrometry,” *Analytical Chemistry*, vol. 90, no. 18, pp. 10943–10950, 2018.

[21] N. B. Hubbard, L. L. Howell, J. P. Barber, D. B. Conkey, A. R. Hawkins, and H. Schmidt, “Structural models and design rules for on-chip micro-channels with sacrificial cores,” *Journal of Micromechanics and Microengineering*, vol. 15, no. 4, pp. 720–727, Mar. 2005.